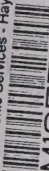


Electronic Services - Hayward, Ca



M19575X



MODEL 2763

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Northeast Electronics at the address below.



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A UNIT OF GENERAL SIGNAL

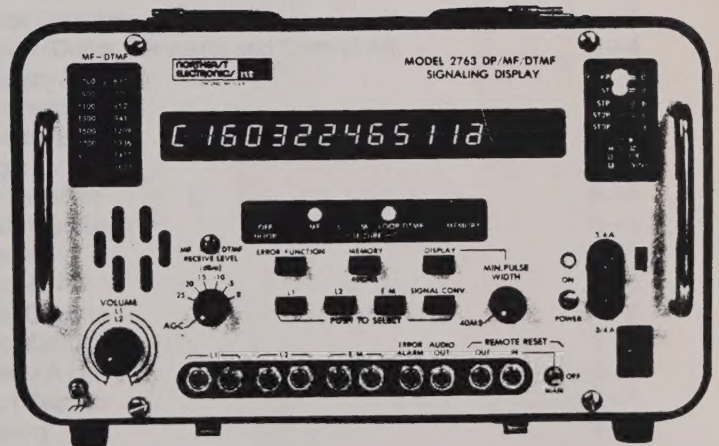
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MODEL 2763 SERIES

DP/MF/DTMF SIGNALING DISPLAYS

SERVICE MANUAL



895 02

Northeast Electronics Instruction Manual
A2763-00-601 Issue 1 August 1982

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SECTION 1

INTRODUCTION

1.1 This manual provides service information for the Northeast Electronics Model 2763 Series DP/MF/DTMF Signaling Displays, including:

- Specifications (Section 2)
- Installation (Section 3)
- Controls, Indicators, and Connectors (Section 4)
- Theory of Operation (Section 5)
- Alignment (Section 6)
- Diagrams (Section 7)
- Electronic Parts Lists (Section 8)

1.2 GENERAL DESCRIPTION

1.3 The 2763 Series Signaling Displays consist of two portable models and a rack-mount model. The portable versions, Model 2763 (pn 2763-00-900) and Model 2763A (pn 2763-02-900), are the same except that Model 2763A does not monitor DTMF signaling. The Model 2763R (pn 2763-03-900) is a rack-mount version of the Model 2763, and is provisioned with rear panel connectors not found on the portable versions.

1.4 The 2763 Series Signaling Displays use high-impedance inputs which can be bridged anywhere on 2-wire, 4-wire, and 6-wire circuits without disturbing normal service. The displays can detect and show DP, DTMF, and MF (CCITT #5 or R1 type) signaling, as well as loop and E&M supervision conditions which include on-/off-hook status, wink, delay dial, answer, and CAMA ANI or TSPS start-dialing events. The signaling displays can also be enabled for detection and diagnosis of signaling pulse timing and amplitude problems. Nearly all monitor, detection, and diagnostic functions of the signaling displays are handled automatically by an internal microprocessor.

1.5 For service observation, a signaling display can be used alone to monitor circuits on an individual "jack-in" basis. Or, the signaling display together with up to three Model 2776 Trunk Access Units provides a fully automatic new-call searching system on up to 90 circuits. In addition, a Model 2765A Call Disposition Analyzer used with the Model 2763R automates its entire service observation and data recording process.

1.6 Detailed application and operational procedures are provided by Northeast Electronics Instruction Manual A2763-00-600; INSTALLATION AND OPERATION.

ARTICLE 1

1.1 The purpose of this document is to provide a clear and concise description of the project and its objectives. It is intended to serve as a reference for all project participants and to ensure that everyone is working towards the same goals. The document will be updated as the project progresses and new information becomes available.

1.2 The project is a multi-phase endeavor that will involve the collaboration of various stakeholders. The primary focus is on the development and implementation of a new system that will improve efficiency and reduce costs. The project is expected to be completed within a six-month timeframe.

1.3 The project is being managed by a dedicated team of professionals who are experienced in project management and have a proven track record of successful project completion. The team will be responsible for the overall coordination and execution of the project.

1.4 The project is a high-priority initiative that is critical to the success of the organization. It is expected that the project will result in significant improvements in the organization's performance and competitive advantage.

1.5 The project is a complex undertaking that requires careful planning and execution. It is essential that all project participants understand their roles and responsibilities and work together to achieve the project's objectives.

1.6 The project is a dynamic environment that is subject to change. It is important that the project team remains flexible and adaptable to any changes that may arise during the project's lifecycle.

1.7 The project is a collaborative effort that requires the active participation of all project participants. It is essential that everyone works together to ensure the project's success.

1.8 The project is a time-sensitive initiative that requires strict adherence to the project schedule. It is important that the project team stays on track and completes the project on time.

1.9 The project is a high-risk initiative that requires careful risk management. It is essential that the project team identifies and mitigates any potential risks to the project's success.

1.10 The project is a complex undertaking that requires a high level of communication and coordination. It is essential that the project team maintains open lines of communication and works together to achieve the project's objectives.

1.11 The project is a dynamic environment that is subject to change. It is important that the project team remains flexible and adaptable to any changes that may arise during the project's lifecycle.

1.12 The project is a collaborative effort that requires the active participation of all project participants. It is essential that everyone works together to ensure the project's success.

1.13 The project is a time-sensitive initiative that requires strict adherence to the project schedule. It is important that the project team stays on track and completes the project on time.

1.14 The project is a high-risk initiative that requires careful risk management. It is essential that the project team identifies and mitigates any potential risks to the project's success.

SECTION 2

SPECIFICATIONS

2.1 The specifications of the Model 2763, 2763A, and 2763R DP/MF/DTMF Signaling Displays are listed in Table 2-1.

Table 2-1. Models 2763, 2763A, and 2763R Specifications.

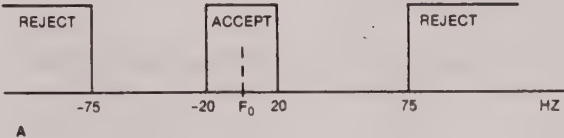
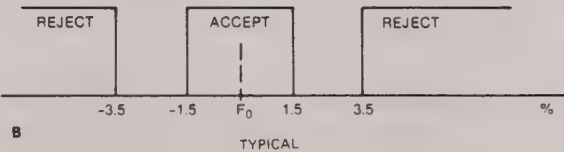
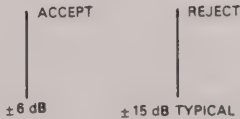
TONE RECEIVER (MF/DTMF)	
SENSITIVITY(dBm into 600 ohms)	
AGC: (Range)	- 26 dBm min. (- 30 dBm typical) + 2 dBm max. (+ 8 dBm typical)
Adjustable: (Range)	- 26 dBm min (- 30 dBm typical) + 2 dBm max. (+ 4 dBm typical)
INPUT IMPEDANCE (L1 & L2)	
Tip to ring:	20 k Ω (200 to 3500 Hz) dc blocked to 100 V
DC INPUT ISOLATION	
Tip to ground, ring to ground:	200 k Ω
FREQUENCY RESPONSE	
MF filter bandwidth:	 A
DTMF filter bandwidth:	 B TYPICAL
TWIST (MF/DTMF)	
(Twist = level difference of the tones in a compound signal . . . high frequency level with respect to low frequency level.)	
Compound level - 20 to + 2 dBm: (MF: F1 and F2 $\pm$ 1% of nominal frequency) (DTMF: F1 and F2 $\pm$ 1.5% of nominal frequency)	 A-02213-00
ACCURACY OF RECEIVE LEVEL CONTROL: (F1 and F2 at nominal frequency)	$\pm$ 2 dB typical

Table 2—1. (Cont'd.)

TONE RECEIVER (MF/DTMF) (Cont'd.)	
ACCURACY OF MIN. PULSE WIDTH	
MF:	± 10 msec
Tone ON: 20 msec to 99 msec	± 5 msec typical with twist ± 1 dB
Tone OFF: ≥ 20 msec (Input level of each frequency component 10 dB or more above RECEIVE LEVEL control setting with no frequency deviation.)	± 7 msec typical with twist = ± 6 dB
DTMF:	± 10 msec
Tone ON: 25 msec to 99 msec	± 5 msec typical with twist $< \pm 1$ dB
Tone OFF: ≥ 25 msec (Input level of each frequency component 10 dB or more above RECEIVE LEVEL control setting with no frequency deviation.)	± 7 msec typical with twist = ± 6 dB
SKEW (MF) ERROR DETECTION: (ERROR FUNCTION enabled)	8 ± 2 msec typical
BALANCE:	Balanced input per PUB 41009
OPTIMUM TALK OFF PROTECTION (DTMF)	RECEIVE LEVEL control set at:
	1. AGC or
	2. at less than 6 dB below input signal.
DIAL PULSE RECEIVER (LOOP)	
SENSITIVITY (DC)	
On hook:	Tip and/or ring more positive than -4 V or open circuit.
Off hook:	Tip and ring more negative than -6 V for more than 10 msec.
NOTE	
Off-hook threshold adjustable from -2 V to -24 V. Factory set at -5.5 V with reference to ground. Typical maximum loop resistance allowable for good operation with factory setting with less than 20 Vrms, 60-Hz longitudinal FEMF.	
CO BATT (Volts)	MAX LOOP RESISTANCE (Ohms)
- 44	1150
- 48	1280
- 52	1400

Table 2—1. (Cont'd.)

DIAL PULSE RECEIVER (LOOP) (Cont'd.)	
PULSE TIMING	
Make period:	10 msec $\leq$ make < 60 msec
Break period:	10 msec $\leq$ break < msec
Off hook (make):	$\geq$ 70 msec
On hook (break):	$\geq$ 235 msec
Interdigital period:	$\geq$ 275 msec
ACCURACY OF MIN. PULSE WIDTH control:	$\pm$ 5 msec
INPUT RESISTANCE	
Tip to ring:	$\geq$ 400 kohms
Tip to ground, ring to ground:	$\geq$ 200 kohms
DIAL PULSE RECEIVER (E&M)	
SENSITIVITY	
Indicated voltages are referenced to CO ground (2763 case)	
E lead on hook:	– 10 V to – 52 V or open
off hook:	more positive than – 8 V
M lead on hook:	more positive than – 8 V
off hook:	– 10 V to – 52 V
INPUT RESISTANCE	
E to ground, M to ground:	$\geq$ 200 kohms
POWER REQUIREMENTS:	117/234 $\pm$ 10 V ac, 50/60 Hz, 25 Watts
ENVIRONMENTAL REQUIREMENTS	
TEMPERATURE	
Operating:	0 °C to 50 °C (32 °F to 122 °F)
Storage:	– 40 °C to 70 °C (– 40 °F to 158 °F)
RELATIVE HUMIDITY:	0 % to 85 %
PHYSICAL CHARACTERISTICS	
Size in case and cover (handles and hinges not included)	36.2 cm l x 21 cm w x 34.3 cm h (14¼ in. l x 8¼ in. w x 13½ in. h)
Weight (in case)	7 kg (16 lb.)

SECTION 3

INSTALLATION

3.1 This section contains information needed for installation and interfacing of the Model 2763, 2763A, and 2763R DP/MF/DTMF Signaling Displays. The information includes:

1. initial inspection (paragraph 3.2),
2. service information (paragraph 3.4),
3. installation of the signaling displays (paragraph 3.9 and 3.11),
4. E&M internal switch settings (paragraph 3.17), and
5. printed circuit board access (paragraph 3.19 and 3.21).

3.2 INITIAL INSPECTION

3.3 The signaling display is carefully inspected, both mechanically and electrically before shipment. It should be working properly when received. If damage from transit is found, notify the transportation carrier immediately.

3.4 SERVICE INFORMATION

3.5 Complete warranty information is contained in the purchase order agreement under terms and conditions of sale. Summarized briefly, the Northeast Electronics warranty extends for a period of one year to the original purchaser of a Northeast test instrument. Northeast's system products are covered by a special warranty which can be summarized as follows.

- ☐ Hardware items are warranted for a period of 90 days.
- ☐ Software is warranted for a period of one year.

3.6 It is recommended that Northeast's Repair Department be contacted for assistance if, for any reason, a Northeast product fails to perform as expected. This step eliminates the needless delay entailed when a product is returned unnecessarily. Contact the Repair Department at Northern Telecom Inc., Northeast Electronics Division, P.O. Box 649, Concord, New Hampshire 03301, telephone: (603) 224-6511.

3.7 If a Northeast Electronics product requires factory servicing **during** the warranty period, be sure to include a ship-to address and a description of the problem when returning the product to Northeast Electronics.

After the warranty period has expired, equipment returned must be accompanied by all of the following:

- ☐ The number of the purchase order covering the cost of servicing,
- ☐ Bill-to address,
- ☐ Ship-to address, and
- ☐ Description of problem.

3.8 In all cases, Northeast Electronics products should be returned directly to our Factory Service Center in Concord, New Hampshire for repair. Any material requiring repair must be returned to Northeast via a Return Material Authorization (RMA) Number, which will be assigned by the Service Center Order Processing Administrator. Customers may call the Factory Service Center at 1-603-224-6511, extension 2257 for the assignment of the number.

3.9 INSTALLING PORTABLE MODELS 2763/2763A DP/MF/DTMF SIGNALING DISPLAYS

3.10 The Models 2763 and 2763A do not require special installation instructions. The signaling displays may be placed on any convenient work surface and connected to a power source (refer to paragraph 4.6). All connections to circuits under test are made via front panel input/output type 310 jacks.

3.11 INSTALLING RACK-MOUNT MODEL 2763R DP/MF/DTMF SIGNALING DISPLAY

3.12 The Model 2763R is supplied with hardware for mounting in a 19-inch (488 mm) rack. A rack mounting bracket (pn C2765-00-109) for installation in a 23-inch (584 mm) rack is available on special order.

3.13 Cooling air intake and exhaust vents located on the rear of the Model 2763R should not be obstructed.

3.14 To mount the Model 2763R in a rack, do the following steps.

1. Remove the two retaining screws located at the rear of the case below the rear panel. These screws hold the chassis secured to the case.
2. Slide the chassis completely out of the case.
3. Fasten the two rack-mount brackets to the sides of the case with 10-32 3/8" long bevel head screws. See Figure 3—1.

4. Install case with brackets in a rack.
5. Slide chassis back into case and secure with the two retaining screws removed in step 1.

NOTE

When installing in a rack, ensure that all cable connections to the Model 2763R have service loops approximately 1½ feet (457 mm) long. This permits pulling the chassis out of the case should service be required from the front.

6. Connect the signaling display to a power source. Refer to paragraph 4.6

7. The signaling display can operate as a stand-alone unit or as part of a signaling test system. See Figure 3—2 and 3—3 for interconnection data when using the Model 2763R in conjunction with Model 2776 Trunk Access Unit(s) and/or Model 2765A Call Disposition Analyzer.

3.15 Connections to circuits under test may be made either via front panel type 310 jacks or a rear panel barrier strip. Figure 3—4 shows the parallel wiring that exists between the front panel jacks and the rear barrier strip.

3.16 When a Model 2763R operates with a Model 2765A Call Disposition Analyzer, the two units are connected to each other via a four-foot cable (pn A2765-00-025). Figure 3—5 shows the pin-out of the external equipment connector jacks and Table 3—1 lists the signals appearing at this jack. The external equipment connector jack is located on the rear of the Model 2763R.

3.17 E&M INTERNAL SWITCH SETTINGS

3.18 The signaling display can accommodate various types of E&M signaling systems. Two dual switches mounted on the line conditioner board configure on-/off-hook detector circuits. Briefly, a detector circuit can be programmed via the switches either as a ground detector (potential more positive than - 8 V) or as a battery detector (potential more negative than - 20 V). In addition, the detector is instructed to interpret the specified state as either an on hook or an off hook.

Figure 3—6 shows the switch locations on the line conditioner board and Table 3—2 lists the resulting on-/off-hook detection requirements set by the switches. Refer to paragraphs 3.19 and 3.21 for instructions to access the line conditioner board in the Models 2763/2763A and Model 2763R respectively.

3.19 PC BOARD ACCESS IN MODEL 2763/2763A

3.20 To obtain access to a board inside the card cage of the Model 2763/2763A, do the following:

1. Shut down the signaling display and disconnect the power cord.

2. Remove the chassis from the case . . . four screws on the front panel and one screw on each side secure the chassis to the case.

3. Locate the pc card retainer bracket (located at the rear of the chassis) and remove the three screws holding the retainer bracket secured to the top edge of the chassis.

4. Remove the retainer bracket to provide free access to the boards inside the card cage.

3.21 PC BOARD ACCESS IN MODEL 2763R

3.22 It is not necessary to remove the Model 2763R from a rack for obtaining access to a board inside the card cage.

1. Shut down the signaling display and disconnect the power cord.

2. Remove the rear panel . . . four screws hold the rear panel secured to the case.

3. Locate the pc card retainer bracket and remove the three screws holding the retainer bracket secured to the top edge of the chassis.

4. Swing the retainer bracket downward to provide free access to the boards inside the card cage.

4-10 X 3/8" S.F. M. SCREWS
(4 PLACES)

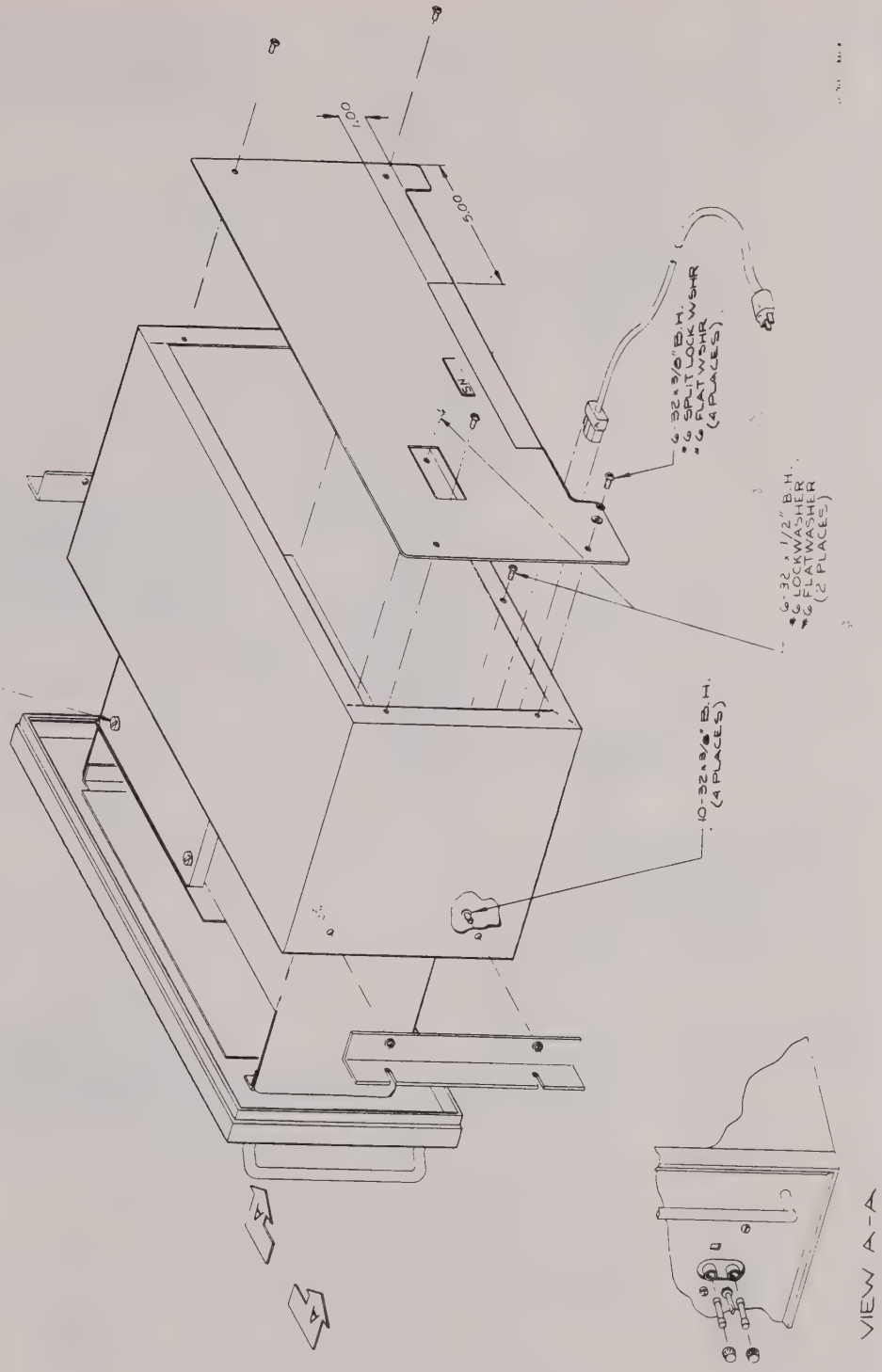


Figure 3-1. Model 2763R Installation Diagram.

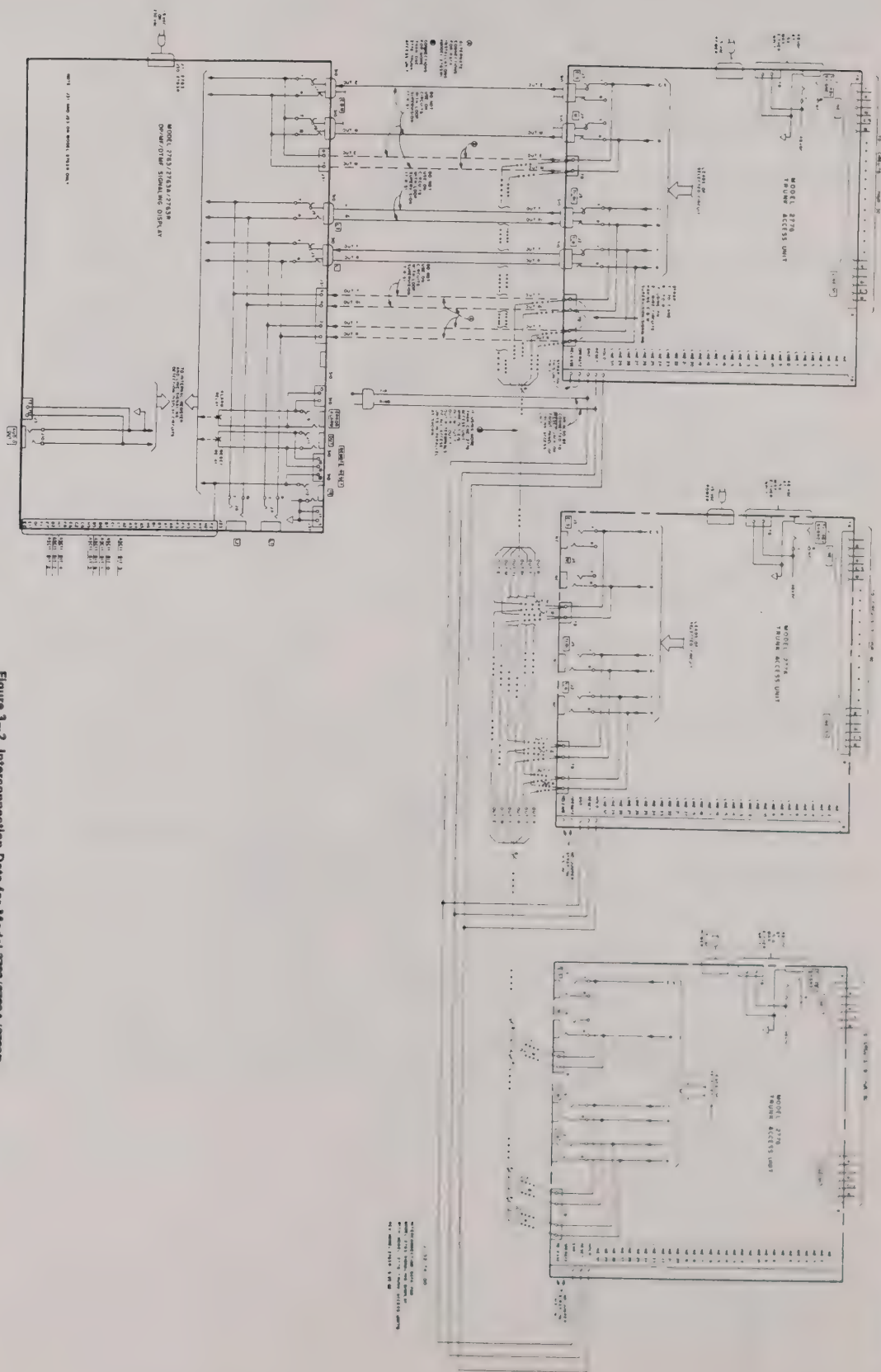


Figure 3-2. Interconnection Data for Model 2783/2783A/2783R Signaling Display with Model 2778 Trunk Access Unit.

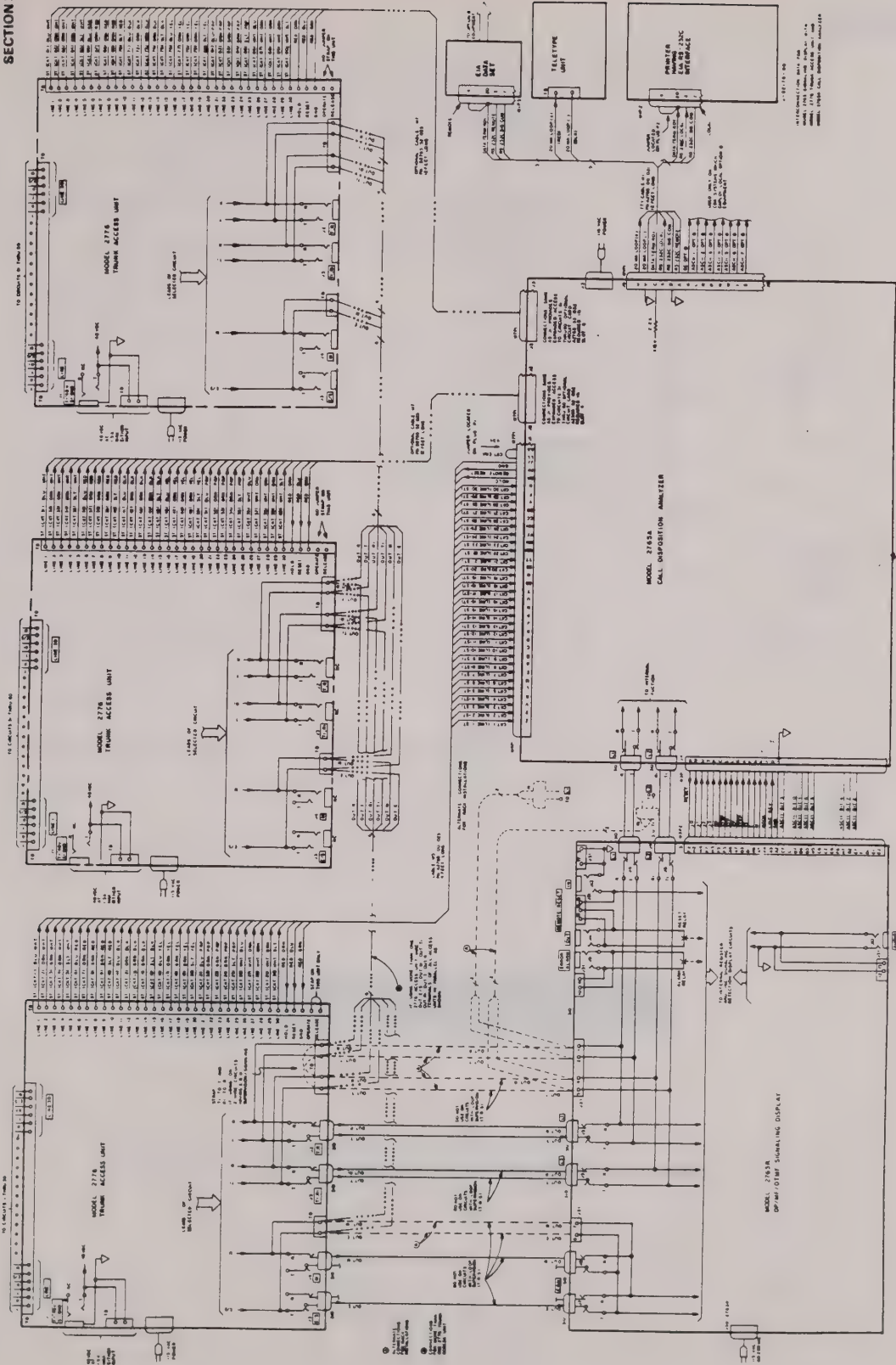
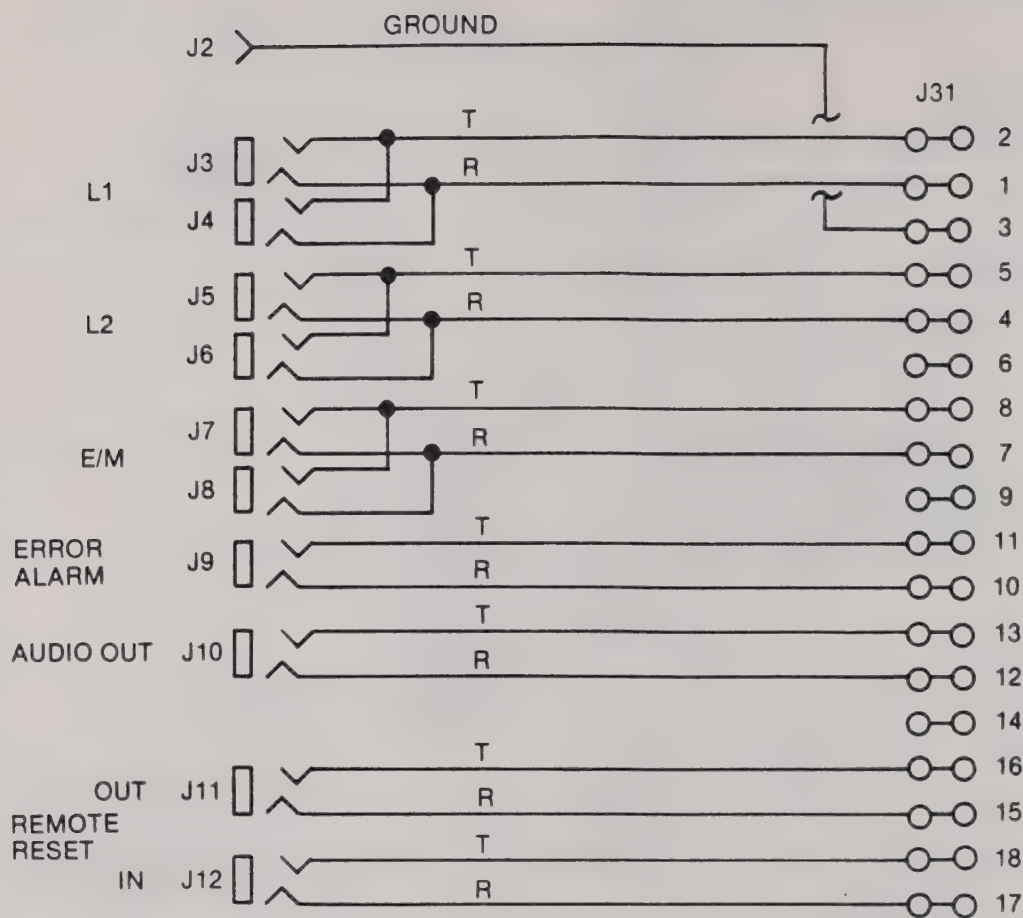


Figure 3-3. Interconnection Data for Model 2763R Signaling Display with Model 2778 Trunk Access Unit and Model 2765A Call Disposition Analyzer.



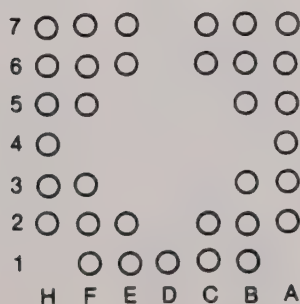
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Figure 3-4. Front Panel to Rear Barrier Strip Interconnection.

Table 3—1. External Equipment Data Bus Signals (Model 2763R).

J23 (33 PINS)	SIGNAL
A2	GND
A3	LINE REV
A4	OFF-HOOK
A5	<u>M</u>
A6	<u>STP</u>
A7	<u>KP</u>
B1	<u>ST</u>
B2	ASCII BIT 7
B3	<u>ST2P</u>
B5	ASCII BIT 6
B6	ASCII BIT 1
B7	ASCII BIT 0
C1	<u>PRINTER DATA READY</u>
C2	NC
C6	NC
C7	ASCII BIT 3
D1	NC
E1	NC
E2	NC
E6	NC
E7	ASCII BIT 2
F1	<u>GND</u>
F2	<u>RESET</u>
F3	<u>ST3P</u>
F5	<u>DP</u>
F6	NC
F7	2^2
H2	2^0
H3	2^3
H4	2^1
H5	ASCII BIT 5
H6	E
H7	ASCII BIT 4



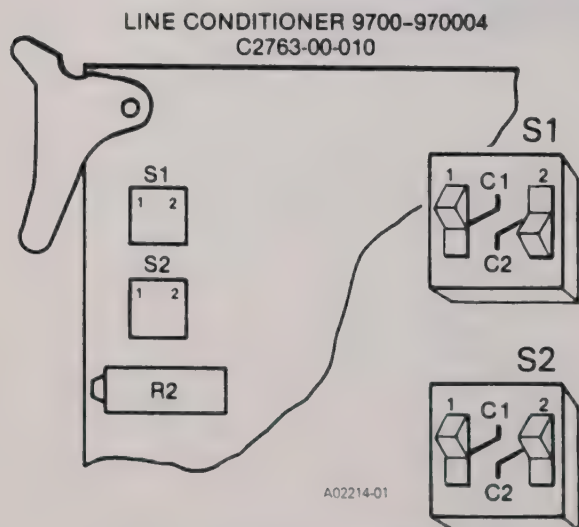
A02215-00

Figure 3—5. Pin-out for External Equipment Data Bus Connector Jack (Model 2763R).

Table 3-2. E&M Internal Switch Settings.

LEAD CONDITION	THRESHOLD SWITCH POSITION	SWITCHING POINT (± 2 V)	INDICATION SWITCH POSITION	INDICATION SHOWN BY A18CR9 OUT = ON HOOK LIGHTED = OFF HOOK
E LEAD	S2-C2		S1-C1	
Battery or open Ground	ON ON	- 8 V - 8 V	ON ON	ON HOOK OFF HOOK
Battery or open Ground	ON ON	- 8 V - 8 V	OFF OFF	OFF HOOK ON HOOK
Battery Ground or open	OFF OFF	- 20 V - 20 V	ON ON	ON HOOK OFF HOOK
Battery Ground or open	OFF OFF	- 20 V - 20 V	OFF OFF	OFF HOOK ON HOOK
M LEAD	S2-C1		S1-C2	
Battery Ground or open	ON ON	- 20 V - 20 V	ON ON	ON HOOK OFF HOOK
Battery Ground or open	ON ON	- 20 V - 20 V	OFF OFF	OFF HOOK ON HOOK
Battery or open Ground	OFF OFF	- 8 V - 8 V	ON ON	ON HOOK OFF HOOK
Battery or open Ground	OFF OFF	- 8 V - 8 V	OFF OFF	OFF HOOK ON HOOK

* Denotes factory switch settings as shown in Figure 3-6.



NOTES.

1. Switch S1 is shown with C1 in the "ON" position, and with C2 in the "OFF" position.
2. Switch S2 is shown with both C1 and C2 in the "ON" positions.
3. For the C1 "ON" position, pins C1 and 1 are shorted (closed).
4. For the C2 "ON" position, pins C2 and 2 are shorted (closed).

Figure 3-6. Internal Switch Locations.

SECTION 4

CONTROLS, INDICATORS, AND CONNECTORS

4.1 This section provides a functional description of controls, indicators, and connectors for the Model 2763 Series DP/MF/DTMF Signaling Displays.

4.2 Figures 4-1 and 4-2 show the front panel controls, indicators, and connectors of Models 2763, 2763A, and 2763R. Rear panel connectors on the 2763R are shown in Figure 4-3. Table 4-1 briefly describes the function of each control, indicator, and connector.

4.3 POWER UP SEQUENCE

4.4 Complete operational procedures are provided by Northeast Electronics Instruction Manual A2763-00-600, INSTALLATION AND OPERATION. A brief power up procedure for the 2763 test set is as follows:

1. Ensure the POWER switch is off.
2. Ensure the 115/230 slide switch matches the power source to be used; either a 115 V ac, 50/60 Hz or a 230 V ac, 50/60 Hz source.

WARNING

For safety reasons it is essential the 2763 test set have an earth ground connection. A proper ground is ensured by either method A or B as follows:

A. Ground connection via power plug

1. Ensure that the third lead of the power outlet connects to earth ground.

2. Do not isolate the NEMA ground lead in the power cord.

B. Ground lug connection

1. Connect the front panel ground lug to a clean frame ground.

3. Remove power cord from the cover compartment and connect it to the power plug. Insert the other end into the power source outlet.

4. Set the POWER switch on and observe the lighted POWER indicator. If the POWER indicator does not turn on, set the POWER switch off and check the input power fuses.

4. Set the POWER switch to ON and observe that the POWER indicator is lighted.

5. Should the POWER indicator fail to turn on . . . set the POWER switch to off and check the fuses.

6. Press the DISPLAY switch and observe that the display shows a number between 20 and 99.

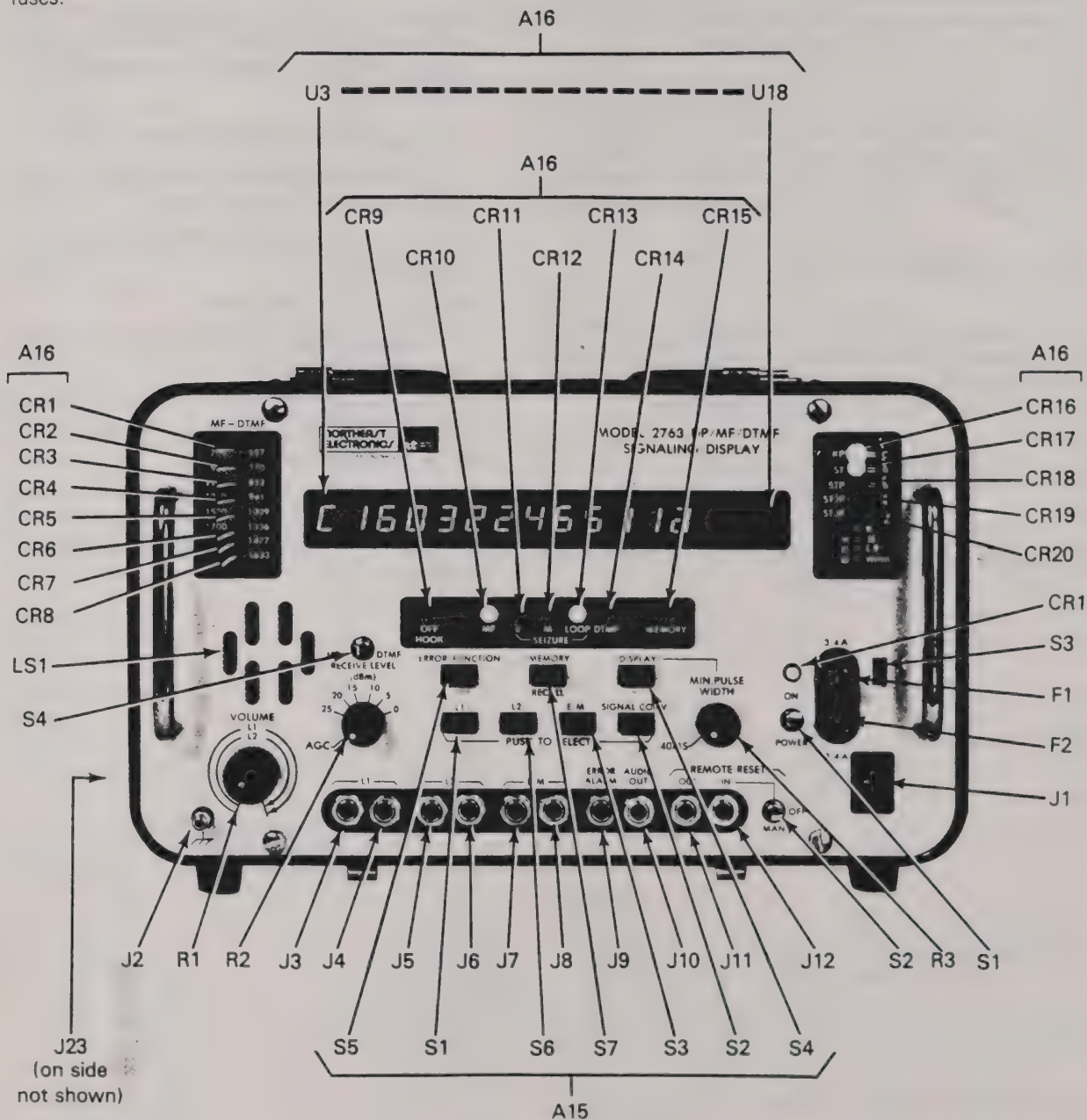
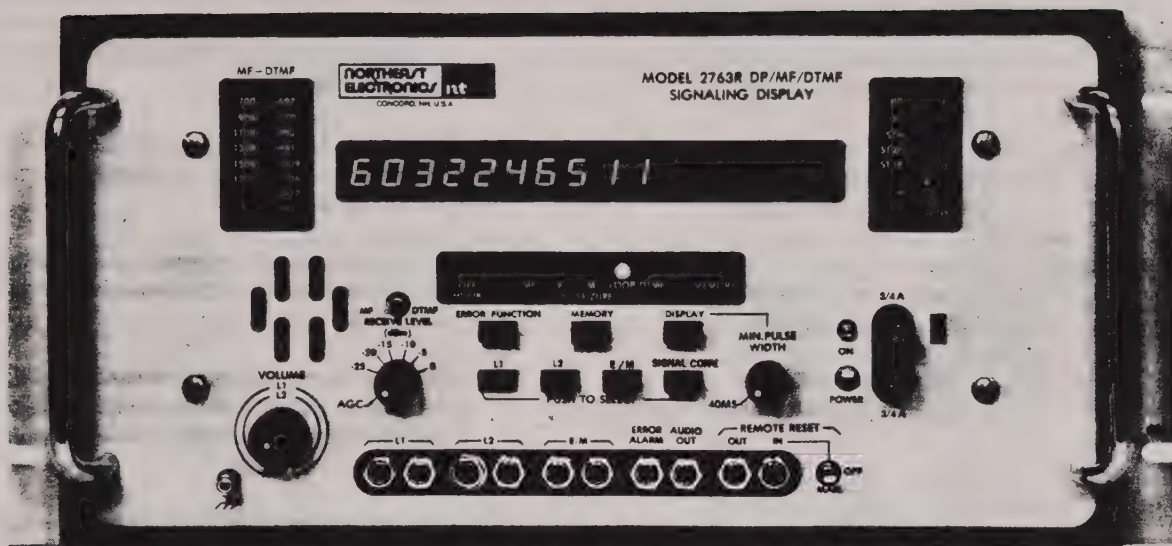
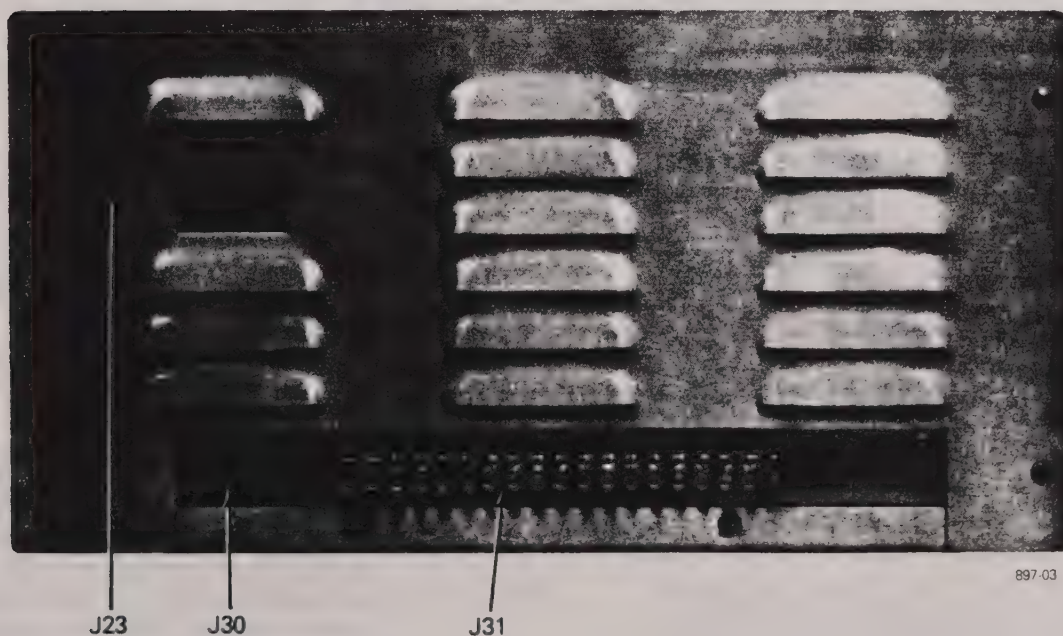


Figure 4-1. Model 2763/2763A Controls, Indicators, and Connectors.



897-02

Figure 4-2. Model 2763R Front Panel Controls, Indicators, and Connectors.



897-03

Figure 4-3. Model 2763R Rear Panel Connectors.

Table 4—1. Controls, Indicators, and Connectors.

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
INPUT / OUTPUT		
J3,J4	L1 phone jacks, mate with type 310 plugs or type 241 twin-plugs	Provides a through connection using a double plug. Bridges the 2763 across a loop circuit under test.
J5,J6	L2 phone jacks, mate with type 310 plugs or type 241 twin-plugs	Provides a through connection using a double plug. Bridges the 2763 across a loop circuit under test.
J7,J8	E/M phone jacks, mate with type 310 plugs or type 241 twin-plugs	Provides a through connection using a double plug. Bridges the 2763 across E/M circuit under test.
J9	ERROR ALARM phone jack, mates with type 310 plug	Provides a contact closure when the 2763 detects an error in the monitored signaling (ERROR function enabled). Contact closure rated at 110 V and 1 A.
J10	AUDIO OUT phone jack, mates with type 310 plug	Provides the combined output of the signal present at input ports L1 and L2. The VOLUME controls set the level at the AUDIO OUT jack.
LS1	Loudspeaker	Provides the audio present on input ports L1 and L2. Sound level depends on input signal levels and VOLUME L1 and L2 control setting.
R1	VOLUME L1, L2 dual concentric potentiometer	Controls the audio level heard on the loudspeaker and signal level present at the AUDIO OUT jack.
J11	REMOTE RESET OUT phone jack, mates with type 310 plug	Supplies a contact closure to reset external equipment. Contact closure occurs on: 1. Manual reset via front panel 2. Reset received from Model 2765A 3. External reset applied at REMOTE RESET IN jack with REMOTE RESET switch set at IN
J12	REMOTE RESET IN phone jack, mates with type 310 plug	Provides an input port to apply a reset signal from external equipment. The 2763 accepts a remote reset signal only if REMOTE RESET switch set is at IN. Reset signal may either be a contact closure between tip and ring or a ground on the tip. All remote resets (accepted internally or not) are repeated and routed as contact closures to the REMOTE RESET OUT jack.

Table 4—1. (Cont'd.)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
INPUT / OUTPUT (Cont'd.)		
J31 (Only on 2763R)	Strip connector	Provides hard-wire termination for permanent installation of a rack-mounted Model 2763R. Contacts on the barrier strip located at the rear of the unit are connected in parallel with front panel input/output jacks J2 through J12. See Figure 4—3.
J23	Accessory output connector	Provides information concerning MF and DTMF data, MF codes and frequencies, data present, and reset supervision including line reversal and off hook. These outputs are intended for use with auxiliary equipment such as Model 2765A Call Disposition Analyzer, printers, and computers.
S2	REMOTE RESET 3-position toggle switch	The connector is located on the left side of the Model 2763, and located at the rear on the Model 2763R. Determines the acceptability of remote reset. OFF position: ignores all remote resets applied either at the REMOTE RESET IN jack or from a Model 2765A CDA. MAN (momentary action) position: initializes internal circuitry. Contact closure applied to REMOTE RESET OUT jack as long as REMOTE RESET switch is held at MAN. IN position: accepts remote resets applied either at the REMOTE RESET IN jack or from a Model 2765A CDA. The remote reset initializes internal circuitry. NOTE The 2763 repeats and routes all remote resets as contact closures to the REMOTE RESET OUT jack regardless of the setting of the REMOTE RESET switch.
DISPLAYS		
A16U3-U18	16-character, 7-segment digit display	Displays available data on a call. . . . either the current call or a call stored in memory as determined by the MEMORY RECALL switch.

Table 4—1. (Cont'd.)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
DISPLAYS (Cont'd.)		
A16CR1-CR8	MF/DTMF light emitting diodes	Displays the MF or DTMF frequencies present at input ports L1 and L2 as identified by the MF or DTMF indicators. When ERROR FUNCTION is enabled, the MF-DTMF LED display latches on the first detected signaling error.
A16CR9-CR15	status LEDs (light emitting diodes)	E,M, LOOP: one of these three LEDs lights up to identify the type of seizure detected . . . if more than one circuit is under test then only the first seizure is displayed. MF, DTMF: one of these two LEDs lights up to identify the type of seizure detected. The lighted LED also identifies the frequency set shown on the MF-DTMF display. OFF HOOK: indicates the on-/off-hook status of the seized circuit under test . . . out for on hook and lighted for off hook. This indicator flashes off and on during dial pulsing on the seized circuit. MEMORY: indicates that the memory has data on a call.
A16CR16-20	MF CODES light emitting diodes	KP: indicates the detection of a "key pulse" during the MF signaling portion of a call with MF/DTMF switch set at MF. ST,STP,ST2P,ST3P: one of these four LEDs lights up to identify the "start pulse" detected during the MF signaling portion of a call with MF/DTMF switch set at MF.
OPERATING MODE CONTROLS		
A15S1	L1 push-push action switch	When in, connects input port L1 to internal measuring circuitry.
A15S6	L2 push-push action switch	When in, connects input port L2 to internal measuring circuitry.
A15S3	E/M push-push action switch	When in, connects input port E/M to internal measuring circuitry.
NOTE When E/M is latched on, the 2763 monitors only the E and M leads for supervision signaling.		

Table 4—1. (Cont'd.)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
OPERATING MODE CONTROLS (Cont'd.)		
A15S2	SIGNAL CONV. push-push action switch	When out, calls are processed sequentially. Data on the current call appears on display while memory holds data on the previous call. When in, two calls are processed in parallel . . . used when testing (DTMF-to-pulse, pulse-to-MF, and MF-to-pulse converters). While testing DTMF to pulse converters . . . DTMF signaling data appears on the display while the pulse signaling data goes to the memory. While testing pulse-to-MF or MF-to-pulse converters . . . pulse signaling data appears on the display while the MF signaling data goes to the memory.
A15S5	ERROR FUNCTION push-push action switch	When in, enables the 2763 to detect and display signaling errors.
A15S7	MEMORY RECALL momentary action switch	When in, the data from memory appears on the display.
A15S4	DISPLAY momentary action switch	When in, the value set for minimum pulse width appears on the display. The value stays on for about two seconds after release of the DISPLAY switch.
R3	MIN. PULSE WIDTH potentiometer type control with detent position	Sets the minimum pulse width threshold for accepting pulses . . . either dial or tone pulses. The selectable range extends from approximately 15 to 99 msec. The detent position sets the minimum pulse width at 40 msec. The 2763 ignores any pulse with a width less than the set value. The display shows the new minimum pulse width anytime the control is set to a new position. The minimum pulse width display remains on for about two seconds after the last detected position change.
S4	MF/DTMF	Enables the 2763 to detect and display either MF or DTMF signaling present at input ports L1 and L2.
R2	RECEIVER LEVEL potentiometer type control with detent position	Sets the minimum acceptable level for MF and DTMF tones. Control range markings are from - 25 dBm to 0 dBm. A detent position provides AGC operation. A 38-dB typical dynamic range with minimum sensitivity of - 26 dBm results in the AGC position.

Table 4—1. (Cont'd.)

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
POWER GROUP		
J1 (Model 2763) J30 (Model 2763R)	ac receptacle	Accepts 115 V ac or 230 V ac to power the 2763.
S1	POWER toggle switch	Applies input power to the 2763.
S3	slide switch	Enables 2763 to accept either 115 V ac or 230 V ac, 50-60 Hz.
F1,F2	¼ A fuses	Protects against excessive input current.
CR1	LED indicator	Lights to show that the unit is powered.
J2	ground lug	Provides access to chassis ground.

SECTION 5

THEORY OF OPERATION

5.1 This section contains two descriptive levels of operational theory. The first is presented at a system block diagram level that relates system electronics to its operational functions and provides a physical breakdown of the circuitry. The second is presented at a system functional diagram level featuring separate circuit functions of the major circuit boards. The system functional diagram includes active component reference designators that allow the reader to apply the text to individual schematic diagrams contained in Section 7.

5.2 SYSTEM BLOCK DIAGRAM DESCRIPTION

5.3 The system operational design of the 2763 Test Set is shown in block form by Figure 7—1. The test set circuitry is grouped under five functional sections:

1. input/output control,
2. signal processing,
3. signaling display,
4. auxiliary equipment interface, and
5. power supply.

5.4 The **input/output control** section determines the monitor and display functions and operational modes of the test set. The input/output control includes the front panel jack ports (together with the rear barrier strip and main power input jack of the Model 2763R) and operating mode controls. Signaling input ports L1, L2, and E/M bridge the test set across external signaling circuits, and the primary signal paths of these ports to the signal processing section are shown with heavyweight lines in Figure 7—1. Secondary control signal paths between other input/output jacks and front panel controls are shown by lightweight lines.

5.5 The **signal processing** function is implemented by a microprocessor-based signaling analyzer with an analog front-end design. The front-end circuitry receives and converts multifrequency and dc signaling to binary formatted inputs that can be processed by the microprocessor circuitry. Multifrequency MF/DTMF tone signaling inputs on the L1 and/or L2 signaling paths are first processed by reception/detection circuitry provided by Main Input A4, MF Detectors A5, A7, and A8, and DTMF Receiver A6 (Models 2763 and 2763R) or Dither Generator and Control A (Model 2763A). The L1 and L2 input signaling paths are

also sent to Line Conditioner A3 which detects loop dial pulse (DP) and supervision. The line conditioner circuitry also detects E&M signaling. Detected signaling data is sent to Microprocessor A11 via the DTMF/MF tone and line status buses. The microprocessor circuitry analyzes received signaling data under operational modes determined by front panel control settings. Processed signaling data outputs via the microprocessor's combined address/data bus.

5.6 The **signaling display** function provides an orderly display of processed signaling data. This functional section is made up of Display Driver A17 and Display Board A16. The display driver board contains logic decoder and driver circuitry needed to interface the address/data bus of Microprocessor A11 to the front panel display components mounted on the display board. The signaling display section also provides signaling information and control together with the microprocessor's address/data bus to the auxiliary equipment interface section.

5.7 The **auxiliary equipment interface** (Model 2763R only) permits use of the 2763 test set with auxiliary equipment such as the Model 2765A Call Disposition Analyzer, printers, and computers. Data inputs from the signal processor and display sections are decoded and buffered by CDA Interface A10 for output to auxiliary equipment via Accessory Board A12. The CDA interface board also provides a contact closure for the error alarm provision of the test set. For portable Models 2763 and 2763A this contact closure is provided by External Alarm Relay Driver A10 which replaces the auxiliary equipment interface.

5.8 The **power supply** function converts externally-applied ac voltage into regulated internal dc voltages. This functional circuit section includes the front panel main power input controls and the internal power supply section shown in Figure 7—1. The front panel 115/230 V ac input is transformer coupled (T1) to Regulator Power Supply A1 which together with regular components VR1 and VR2 generate the dc voltages used by the system electronics. The supplied dc voltages are designated + / - 12 V REG, + 5 V REG, and + 5 V REG (DISPLAY). The + 5 V REG (DISPLAY) is used within the signaling display section only, while the remaining dc voltage outputs are distributed as required throughout other functional sections.

5.9 Physically, the functional block sections of Figure 7—1 are distributed in both front and rear panel

assemblies of the 2763 test set. The input/output control and signaling display sections are housed in the front Sub-Panel Assembly A19. This front panel assembly also mounts the 115/230 V ac main power input control components. (The Model 2763R has its power jack mounted on the rear panel assembly.) The signal processor, auxiliary equipment interface, and internal power supply sections are housed in rear Card Cage Assembly A14. This front and rear distribution is best shown by Figure 7—4. As shown, the input/output jacks and operator controls contained within Sub-Panel Assembly A19 connect to rear Card Cage Assembly A14 via cables W1 and W2. The signaling display section, identified by Display Assembly A18, connects to the rear assembly via cable W3. The three cables (W1, W2, and W3) connect to Interconnect Board A13 of the rear cage. As implied, the interconnect board provides interconnections between plug-in circuit boards contained within the card cage.

5.10 The interconnections between Interconnect Board A13 and the plug-in circuit boards of the card cage are shown by Figure 7—8. The plug-in circuit boards together with Microprocessor A11 make up the signal processor section. Regulator Power Supply A1 and CDA Interface A10 or External Alarm Relay Driver A10 are also plug-in circuits housed within the card cage.

5.11 SYSTEM FUNCTIONAL DIAGRAM DESCRIPTION

5.12 MAIN INPUT A4

5.13 Main Input A4 divides into three functional sections:

1. multifrequency signal processing,
2. audio reproduction, and
3. remote reset control.

5.14 Multifrequency Signal Processing

5.15 Signaling appearing on the L1 and L2 input jacks is monitored by the two high-impedance, dc-blocked transformers T1 and T2. Dual amplifier U4 provides signal isolation, and balance adjust R15 is set for a balanced amplification of both signaling channels. Front panel PUSH TO SELECT switches L1 and L2 then determine whether only one or both signaling channels are applied to summing amplifier U1. When channel L1 is selected, electronic switch Q1 is enabled, and when L2 is selected, electronic switch Q2 is enabled. The two signaling channels are linearly summed by amplifier U1 when both Q1 and Q2 are enabled. Input gain adjust R1

sets the initial overall gain of the summed channels. After the first valid digit signal is processed by the test set, the gain of the summing amplifier is raised approximately 3 dB by a low HYST-GAIN input controlled by Microprocessor A11. This added hysteresis gain prevents signal dropout if the input signaling level drops slightly once signaling is detected.

5.16 The summing amplifier output is filter limited before separation into DTMF and MF signal paths to the receiver/detector circuitry. The prefilter circuit (U3 and U6) limits the input composite frequency spectrum to a 700- to 3k-Hz bandwidth. Configured from VCVS (voltage-controlled voltage source) networks, the filter circuitry provides unity gain with a 24-dB low end roll-off and a 12-dB high end roll-off. The DTMF signal output is taken directly from the filter output, while the MF signal output is attenuated by a 6-dB pad (R52 and R53).

5.17 In addition to the DTMF and MF output signal paths, the output of the bandpass filter is monitored by a peak level detector circuit (U6A and Q8). The peak detector is a charge and hold circuit which detects the negative peak level output of the filter and generates a dc signal level proportional to the received composite signal level. The generated dc level is developed across a voltage divider network that determines the dc signal level output of Main Input A4. The resistance configuration of the divider network is controlled by the front panel MF/DTMF toggle selector S4. For the DTMF position of toggle S4, the output signal level is typically 0.04 to 0.9 V dc (approximately 0.75 V dc for a composite signal input at L1 or L2 of 0 dBm). The MF position of toggle S4 lowers the output signal level approximately 0.06 V dc. The dc signal level output from Main Input A4 is applied to the front panel RECEIVE LEVEL control R2 and is used to provide MF/DTMF signal level control when R2 is set for AGC operation.

5.18 Audio Reproduction

5.19 The transformer-monitored signaling of the L1 and L2 inputs is processed by the audio reproduction circuits which provide audio signal outputs to the front panel speaker and AUDIO OUT jack. The L1 and L2 signal paths are applied to separate highpass filters U5A and U5B, and then amplified by U2A and U2B. The amplifier outputs are developed across voltage dividers incorporating front panel L1 and L2 VOLUME control R1. Control R1 contains dual concentric potentiometers which control the audio level heard at the loudspeaker and the signal level present at the AUDIO OUT jack. The volume-controlled signals are then summed, amplified, and routed to speaker LS1 and connected to the AUDIO OUT jack.

5.20 Remote Reset Control

5.21 The remote reset control of Main Input A4 provides a relay contact closure to reset external equipment via the front panel REMOTE RESET OUT jack. The contact closure is caused by a relay driver circuit which operates in association with the front panel REMOTE RESET toggle switch S2. Switch S2 controls the internal SYS RES signal applied to Microprocessor A11. The relay driver circuit receives a low reset input from the REMOTE RESET IN jack, or from the manual position of the S2 toggle switch. A low signal from either source causes the relay driver circuit to short the tip and ring leads of the REMOTE RESET OUT jack. The reset input from the REMOTE RESET IN jack is sent by external equipment which may cause either a tip and ring closure, or apply a ground to the input tip lead. The input tip path of the Model 2763R is OR-wired to the CDA RES IN path of CDA Interface A10 so that the external reset signal may be sent by a Model 2765A Call Disposition Analyzer. In either case, a received REM/CDA RES signal is applied across R44 to the relay driver circuit and to switch S2 as a EXT RES signal. When S2 is set to its IN position, the EXT RES signal outputs S2 as a low SYS RES signal to Microprocessor A11. When switch S2 is placed in its MAN position, a low MAN RES signal is applied to the relay driver circuit of Main Input A4. The MAN position also outputs a SYS RES to Microprocessor A11.

5.22 MF DETECTOR A5, A7, AND A8

5.23 Three MF circuit boards are used to provide six separate detector circuits for the processing of a two-of-six multifrequency (MF) pulse signaling system. An MF code consists of two different frequencies taken from six possible frequencies: 700-, 900-, 1100-, 1300-, 1500-, and 1700-Hz tones. Each detector circuit is tuned to one of the six possible frequencies, and processes the composite MF signal input from Main Input A4 for the presence of its associated single tone. A detected tone burst is converted to a digital pulse output, and the six detector outputs together make up the two-of-six, binary formatted MF signal input analyzed by Microprocessor A11. The combined MF tone output is routed through DTMF Receiver A6 (Model 2763 and 2763R) or Dither Generator and Control A6 (Model 2763A) to the DTMF/MF tone bus of Microprocessor A11.

5.24 Each detector circuit consists of a broadband filter, hard limiter and trailing edge detector circuits, a narrowband filter, and a tone presence detector. The detector circuits operate the same way, except for separate frequency identities.

5.25 Broadband Filter

5.26 The broadband filter further limits the MF signal spectrum received from Main Input A4. The filter net-

work is a generalized immittance circuit configured for a 100-Hz bandwidth centered on its respective tone of interest. The filter's output is applied to the hard limiter and trailing edge circuit.

5.27 Hard Limiter

5.28 The hard limiter receives the broadband filter output and a dither signal level control input. The dither signal is a positive level, 16-kHz square wave and controls the threshold of the hard limiter. The dither level is sent from DTMF Receiver/Dither Generator and Control A6, and its positive pulsed level is determined by the front panel RECEIVE LEVEL control R2. For tone detection the dither level must be significantly less than the broadband filter input to the hard limiter. When the filtered signal input is significant when compared against the level of the dither signal, the hard limiter suppresses the dither input and passes the filtered input signal. If the filter input level is not significant, the dither signal captures the limiter.

5.29 The limiter outputs a pulsed constant level signal with a frequency determined by the dominate input signal frequency—either 16 KHZ for a dominate dither input, or at a frequency equal to the filtered input. The limiter's output is applied to a U2 gate controlled by the trailing edge detector.

5.30 Trailing Edge Detector

5.31 The trailing edge detector monitors the output of the broadband filter to produce a positive control pulse during the presence of a received tone burst. The positive pulse is used to gate the hard limiter output to the narrowband filter, and to disable the tone presence detector at the end of a tone burst. The trailing edge detector consists of an envelope (U6) and level decay detector (U7). The resultant positive pulse follows the absolute value of the filtered tone burst and ends when the trailing edge of the tone burst waveform drops 2 dB. While the positive pulse is present, the hard limiter's output is applied to the narrowband filter, and the tone presence detector is enabled.

5.32 Narrowband Filter

5.33 The narrowband filter is the last frequency discrimination circuit for tone detection. The filter is a generalized immittance circuit configured for an output bandwidth of 80 Hz centered on its frequency of interest. Potentiometers R47 and R26 are used for alignment of the center frequency and bandwidth. When a tone burst is detected the narrowband filter outputs a series of positive TTL level pulses at the same frequency rate of the detected tone burst.

5.34 Tone Presence Detector

5.35 The tone presence detector converts the tone burst output of the narrowband filter to a positive logic output with a pulse duration that represents the duration of the tone burst. The tone presence detector is a retriggerable, one-shot multivibrator network which is triggered and retriggered for the duration of a detected tone burst. The tone presence detector is disabled at the end of the tone burst by the trailing edge detector circuit. This conversion is the end of MF analog processing, and digital processing commences with the tone presence detector output lines of all six MF detector circuits being presented to Microprocessor A11.

5.36 DTMF RECEIVER/DITHER GENERATOR AND CONTROL A6

5.37 The DTMF receiver board is used with rack-mount Model 2763R and portable Model 2763. Its primary function is to detect DTMF tone signaling. In addition, it generates a dither signal used to control the signaling sensitivity of the MF detector boards. Also, detected MF tone outputs are routed through the DTMF receiver board when the Model 2763R or Model 2763 is enabled for the MF signaling mode of operation.

5.38 The Model 2763A does not provide a DTMF signaling mode of operation. In the Model 2763A the DTMF receiver board is replaced with the dither generator and control board which functions to provide the dither signal used for sensitivity control of the MF detector boards. Also, detected MF tone outputs are routed through the dither generator and control board.

5.39 The primary difference in circuitry between the DTMF receiver board and the dither generator board is that the dither board is devoid of DTMF detection and control circuits, as well as output switching circuits used to differentiate between an enabled MF or DTMF signaling mode of operation. The dither generator circuits of the two boards are essentially the same. Therefore, the dither circuit of the dither generator and control boards is treated in the discussion of the DTMF board under the dither generator circuit section.

5.40 The DTMF receiver board circuits are grouped as follows:

1. low/high group filter,
2. level discriminator,
3. threshold comparator,
4. steering logic,
5. DTMF tone detector,
6. DTMF/MF output control, and
7. dither generator.

5.41 Low/High Group Filter

5.42 A DTMF signal code contains two different frequencies. The lower frequency is selected from a group of four low tones (697, 770, 852, and 941 Hz), and the higher frequency is taken from a second group of high tones (1209, 1336, 1477, and 1633 Hz). The DTMF receiver board has separate filter receiver channels for the detection of a signal's low and high frequency content.

5.43 The low and high group filter channels further limit the frequency spectrum received from Main Input A4. Each filter outputs its respective group band of interest with a 0-dB gain. The filters have an out-of-band rejection greater than 40 dB which eliminates dial tones (350/440 Hz) and permits detection of digit codes in the presence of dial tone. The low and high group filtered outputs are applied to the level discriminator and threshold comparator circuits.

5.44 Level Discriminator

5.45 Each group filter channel uses a level discriminator circuit to enable its threshold comparator circuit. When the output level of the group filter is greater than 32 mV RMS, the discriminator initiates a high enabling output consisting of repeated positive pulses generated for successive negative periods of the input signal to the level discriminator. The level discriminator also quickly detects the end of the received tone burst, and the resultant positive enabling pulse lasts only slightly longer than two cycles of the lowest frequency of the filtered group frequency (697 Hz for the low group, and 1209 Hz for the high group). Consequently, the level discriminator enables the threshold comparator only for the duration of the tone burst period, reducing the effects of filter ringing and the filter output's exponential decay period.

5.46 Threshold Comparator

5.47 The threshold comparator circuit is enabled during the presence of a received tone burst by the level discriminator circuit. The threshold level of the comparator circuit is determined by the front panel RECEIVE LEVEL control R2. For the AGC detent position of control R2, the threshold level is determined by the signal level control input from Main Input A4. For the -25 to 0-dB range positions of control R2, the threshold level is set by a voltage divider network controlled by R2. The threshold comparator compares the group filter output level against the threshold level. When the compared signal level is greater compared to the threshold level, the comparator outputs a positive pulse for each cycle of the input signal.

5.48 The pulse rate of the comparator's output pulse train equals the frequency of the received input signal.

The output of the comparator circuit is routed by the steering control to the respective high or low frequency port of the DTMF tone detector.

5.49 Steering Logic

5.50 The steering circuit controls the application of received group frequencies to the DTMF tone detector circuit. For DTMF tone detection, the tone detector must receive signal inputs at both its high and low frequency ports. Signaling present on only one of the tone detector ports is ignored by the tone detector circuit. When the front panel ERROR FUNCTION control (S5) is enabled for single-tone error detection, the steering circuit provides signal inputs to both high and low ports of the tone detector when a single-tone error is received.

5.51 Normally, the steering circuit monitors both threshold comparators and routes each received group frequency signal only to its respective high or low port of the tone detector. When enabled by a low $\overline{\text{ERR FUNCT}}$ control signal at pin K of P6 (ERROR FUNCTION enabled), the steering circuit still routes both frequency signals of a valid DTMF tone to associated high and low tone detector ports; however, when a single-frequency error condition is received, the received single frequency is routed to both high and low ports of the tone detector. With signaling present on both its input ports, the tone detector is able to detect a single-tone error condition.

5.52 DTMF Tone Detector

5.53 The DTMF tone detector is a CRC 8030 LSI chip dedicated to DTMF tone detection. The detector provides a two-of-eight binary output format, where two of eight frequency lines are set to a logic low, indicating the high and low frequencies in a detected DTMF tone.

5.54 To function, the tone detector requires signal inputs at both its FL and FH input ports. Normally, the tone detector receives these two signals from both threshold comparators via the steering circuit. Each signal is in the form of a square wave pulse train with a pulse rate equal to the received group signal frequency, and each pulse train is steered to its respective FL or FH input. The tone detector monitors both FL and FH input signals and sets two of its eight output lines low to indicate a valid DTMF tone code.

5.55 When the front panel ERROR FUNCTION control is disabled, the tone detector ignores a single group frequency input (FL or FH), and all of its eight output lines remain at a logic high. When the ERROR FUNCTION control is enabled and a single-frequency error condition exists, the received group frequency is applied to both FL and FH inputs, allowing the tone detector to indicate the single-frequency error condition by setting

a logic low on the appropriate frequency output line. Should a received DTMF code signal consist of three frequencies (for example, a signal consisting of one low-group frequency and two high-group frequencies), the detector decodes the single group frequency but ignores the combined frequency port input (received at the FH port for the given example), and sets the appropriate frequency output line to a logic low.

5.56 The eight DTMF tone detector outputs are further processed by Microprocessor A11 which determines the final acceptance and display of valid DTMF tones and signaling error conditions. The tone detector outputs are switched onto the processor's DTMF/MF tone bus via the DTMF/MF output control circuit.

5.57 In addition to frequency detection, the DTMF tone detector outputs a 16-kHz signal to the dither signal generator circuit.

5.58 DTMF/MF Output Control

5.59 The DTMF/MF output control circuit consists of two multiplexer circuits controlled by the front panel MF/DTMF toggle switch. For the toggle's DTMF position, a logic high at P6, pin 8 causes the output control to switch the DTMF tone detector outputs onto the DTMF/MF tone bus input to Microprocessor A11. The MF tone inputs from the MF detector boards are switched onto the DTMF/MF tone bus when the toggle switch is set to its MF position.

5.60 Dither Generator

5.61 The dither generator circuit provides a receiver sensitivity control signal to the MF detector boards. The dither generator circuit on DTMF Receiver A6 uses a 16-kHz output from the DTMF detector circuit to chop the dc level REC LEVEL input at pin H of P6 into a 16-kHz dither signal output with a 50% duty cycle. The dither generator circuit on Dither Generator and Control A6 uses the $\overline{\text{ALE}}$ signal input at P6, pin J to generate the dither signal. The $\overline{\text{ALE}}$ signal input is applied to a divide-by-32 counter network, the output of which is used to chop the REC LEVEL input into a 13-kHz dither signal with a 50% duty cycle. The level of the dither signal from either generator circuit provides the receive sensitivity control at the MF receiver boards.

5.62 LINE CONDITIONER A3

5.63 In general, Line Conditioner A3 monitors the dc level of the loop (L1, L2) and E&M signal paths, and conditions detected signal states for the line status bus input to Microprocessor A11. The line conditioner board contains two (L1 and L2) monitor circuits for loop signal conditioning and two (E and M) monitor circuits for E&M signal conditioning. Because these circuits

monitor polarity changes on external telephone circuit leads, the ground circuit of Line Conditioner A3 must connect to the ground reference of the circuits under test to ensure proper operation.

5.64 Loop Monitor Circuits

5.65 The L1 and L2 monitor circuits are identical, and each monitor circuit divides into a line reversal detector channel and an off-hook detector channel. Before application to the two channels, both tip and ring level inputs to the monitor circuit are attenuated 6 dB and limited between 0 and -12 V dc.

5.66 The line reversal channel detects polarity reversals between tip and ring. With an open circuit, or on-hook condition, the tip input to the line reversal detector is more positive than the ring, and the detector outputs a low (0 V) logic state signal. The detector channel considers a tip-ring reversal to occur when the tip becomes more negative than the ring, and indicates this condition with a high (+ 5 V) logic state signal, L1 REV (or L2 REV).

5.67 The off-hook detector channel includes a 60-Hz rejection circuit and an open circuit detector circuit. The off-hook circuit compares both tip and ring dc levels against a common reference set by the on-board threshold adjust R2. (Note that R2 sets the dc sensitivity for both the L1 and L2 front panel ports.) When both tip and ring dc levels at the L1 (or L2) input port are more negative than -6 V, the off-hook detector causes a low (0 V) logic output (L1 OFF HK or L2 OFF HK) to the line status bus. To signal an on-hook condition, where the port tip and/or ring are more positive than -4 V, the off-hook detector causes a high (+ 5 V) output to the line status bus. Dial pulse port inputs are indicated by a train of positive pulse outputs from the line conditioner board. When tip and ring lead connections to a front port are removed the open-circuit detector causes a low logic output (L1 OFF HK, or L2 OFF HK) for approximately 500 msec, then returns the output line to a + 5 V state.

5.68 The 60-Hz rejection portion of the off-hook detection channel blocks the effects of stray 60-Hz signaling which might be present at the input ports. For each detected tip and ring level condition, the rejection circuit presents a high or low limit blocking threshold to prevent 60-Hz interference with an indicated on/off-hook condition. The required limit thresholds are provided by the on-board high adjust R43 and low adjust R44, which are factory set to block the interference of a 20-Vrms, 60-Hz longitudinal FEMF.

5.69 E&M Monitor Circuits

5.70 The line conditioner board provides separating conditioning channels for E and M lead input signals.

Two on-board dual switches allow the channels to accommodate various types of E&M signaling systems. Each channel can be programmed by the switches, either as a ground detector (input potential more positive than -8 V) or as a battery detector (input potential more negative than -20 V). Also, the switches instruct the circuit to interpret the specified state as either an on-hook or an off-hook condition.

5.71 The S2C2 threshold switch of the E lead conditioning channel is factory set for ground detection, and the S1C1 indication switch is set to indicate a ground condition with a low (0 V) logic signal, E OFF HK. A battery, or open-circuit port condition, is indicated by a high (+ 5 V) output. Dial pulsing present on the E lead is indicated by a series of positive pulses.

5.72 The S2C1 threshold switch of the M lead conditioning channel is factory set for battery detection, and the S1C2 indication switch is set to indicate a battery condition with a low (0 V) logic signal, M OFF HK. A ground, or open-circuit port condition, is indicated by a high (+ 5 V) output. Dial pulsing present on the M lead is indicated by a series of positive pulses.

5.73 MICROPROCESSOR A11

5.74 Microprocessor A11 provides the intelligence required to analyze detected signaling data for an orderly presentation of information. It determines the final acceptance or rejection of monitored signaling as well as the information displayed, or used by equipment external to the test set. In rack-mount Model 2763R and portable Model 2763, Microprocessor A11 receives detected ac signaling data via DTMF Receiver A6. For portable Model 2763A, ac signaling data is received via Dither Generator and Control A6. In all models, Line Conditioner A3 provides Microprocessor A11 with detected dc polarity and pulsing data. Received signaling data is analyzed and processed for display in response to operational mode data provided by the front panel control settings. Microprocessor A11 outputs signaling information via a combined address/data bus to Display Assembly A18. In Model 2763R, this microprocessor bus also inputs CDA Interface A10.

5.75 Microprocessor A11 uses a single-chip microcomputer with expanded memory and associated read/write control circuits. This microcomputer circuitry, together with reset interrupt and minimum-pulse width circuitry, implement the data processing functions of Microprocessor A11. The signal processing functions of Microprocessor A11 are discussed in terms of the microcomputer operations and accompanying reset and interrupt control circuits.

5.76 Input/Output Section

5.77 Three 8-bit ports and three single-line inputs of the microcomputer are used for input and output functions. Signaling data input functions are assigned to Port 1, the upper half (P24-P27) of Port 2, and to test input T0. The other single-line inputs, $\overline{RES}$ and $\overline{INT}$, monitor reset and interrupt control signals. Port 0 (or BUS), together with the lower half (P20-P23) of Port 2, make up the combined address/data bus used to access memory and data registers external to the microcomputer.

5.78 The $\overline{MF/DTMF}$ control input at P24 of Port 2 determines the MF or DTMF processing mode of the microcomputer. The MF or DTMF tone data received at Port 1 carries the tone duration and frequency content analyzed and decoded by the microcomputer into digit/code data outputs.

5.79 Line status data is received at input T0 through the 8-channel multiplexer switch controlled by lines P25-P27 of Port 2. The three Port 2 binary lines to the multiplexer switch only one of the eight status lines at a time for input to the microcomputer. The data input at T0 is analyzed and decoded by the microcomputer into supervision and dial pulse conditions present at the L1/L2, or E&M input ports.

5.80 The operating mode of the microcomputer for monitoring and processing DTMF/MF tone and line status signaling data is provided by the on-board FPS and MPW data registers. The FPS data register holds the operating mode status established by the seven front panel PUSH TO SELECT switches and the detent 40MS position of the MIN. PULSE WIDTH control. A 15 to 99-msec range selection of the MIN. PULSE WIDTH control is held in the MPW data register. Data from these registers enters Port 0 of the microcomputer, and is accessed via the combination memory/I/O circuitry external to the microcomputer chip.

5.81 Two other control inputs to the microcomputer appear at the $\overline{RES}$ and $\overline{INT}$ inputs. The $\overline{RES}$ signal input is provided by the reset control circuit which provides a low (0 V) logic pulse of sufficient duration to reset the internal circuitry of the microcomputer. The $\overline{RES}$ signal is produced at system power-up, or originates from a converted $\overline{SYS RES}$ input to the reset control circuit. The $\overline{SYS RES}$ signal is received from the front panel's REMOTE RESET IN switch. The reset control also resets the interrupt generator and the MPW control circuits.

5.82 The $\overline{INT}$ inputs to the microcomputer are generated at a 1-msec nominal rate set by on-board potentiometer R7. The generated interrupts notify the microcomputer when to update the front panel's 16-digit display, and to check internal software event timers. The interrupt pulses are also used as clock

inputs by the MPW control circuit. The interrupts clock the MPW control circuit during a period of time set by the MIN. PULSE WIDTH control to produce a BCD representation of the minimum pulse width threshold. After the threshold value is clocked, the MPW control also outputs a latching signal which stores the BCD coded output in the MPW data registers.

5.83 Processed data outputs the microcomputer via Port 0. This 8-bit output port (PB0-PB7) is inverted and buffered to provide the output bus ($\overline{PB0-PB7}$) of Microprocessor A11. In addition to this processed data output, the microprocessor board outputs four control signals, $\overline{PRINTER DATA}$, $\overline{HYST GAIN}$, $\overline{ALE}$, and $\overline{WRD}$. The printer data signal is used by Model 2763R to notify external printer equipment that ASCII data is present on the microprocessor's output bus. The hysteresis gain output is used as a receive gain control in Main Input A4. The remaining $\overline{ALE}$ and $\overline{WRD}$ outputs are used to access display and external data control circuits of Display Assembly A18.

5.84 Data Processing

5.85 Data input, processing, and output functions of Microprocessor A11 are governed by the microcomputer, which operates under software instructions and data programmed in memory locations, both internal and external to the microcomputer. With the exception of an external crystal reference, the timing generation for microcomputer instruction cycles is self-contained.

5.86 After a power-on or external reset, the microcomputer begins main program routines which control data input and processing. The microcomputer's interrupt input is enabled as part of the main program operation. The interrupt generator applies interrupt signals to the microcomputer's $\overline{INT}$ input at a 1-msec rate. An interrupt signal causes the microcomputer to temporarily depart from a main program routine and to refresh a display digit. The microcomputer also uses the generated interrupts as clocking pulses to update software event timers located in memory. After performing an interrupt routine, the microcomputer returns to the interrupted main program routine and continues a cyclical main program operation which controls the monitoring of signaling and front panel control data. The operational status of the front panel determines what types of signaling data (MF/DTMF and/or Loop/E&M) are monitored and how they are processed. Software event timers in RAM memory are started, clocked by the 1-msec interrupts, and stopped as various signaling conditions and events are analyzed and decoded.

5.87 Memory and I/O Expansion

5.88 Use of the lower half (P20-P23) of Port 2 with the address functions of Port 0 (BUS) provides the

microcomputer's 12-bit address bus which is used to access external memory and I/O circuits. The microcomputer contains 1k words of program memory and 64 words of data memory. In addition to this resident memory, 4k words of program memory are provided by ROM U25, and 256 words of data memory are provided by RAM circuits U10 and U16.

5.89 The microcomputer uses two enabling signals (ALE and PSEN) and its read/write outputs together with the 12-bit address bus to access external memory. The ALE (address latch enable) signal is used with addressing either program or data memory, but read/write data memory operations are separate from program memory addressing. The PSEN (program store enable) output occurs only during program memory addressing, and a read/write output occurs only during data memory addressing.

5.90 All program memory fetches less than 1024 occur internally with no external signals being generated (except ALE which is always present). At address 1024 (400 hex), external program memory fetches are initiated, and the 12-bit address is latched internally by ALE on Port 0 and the lower half of Port 2. The 12-bit address is also latched by ALE in the address and control-bit registers which determine how the ROM memory is accessed. The address registers apply only 11 bits (PB0-PB10) to the 12-bit address input of the ROM memory. Address bit PB11 is set independently of the other bits by programmed software instructions, and is applied to ROM memory by the control-bit register. The separate setting and control of PB11 allows the microcomputer to address all 4k of ROM memory. Only 4k of program memory is directly addressed by the microcomputer's program counter. These directly accessed addresses include the 1k resident program memory (000 to 3FF hex) and the last 3k of ROM memory addresses (400 to 7FF, 800 to BFF, and C00 to FFF hex). The first 1k of ROM memory (000 to 3FF hex) is indirectly accessed by forcing PB11 (P23 of Port 2) low when the microcomputer's program counter is set to an address in block 800 to FFF hex. The external address presented to the ROM memory then accesses the ROM's first 1k of memory (000 to 3FF hex). The PSEN (program store enable) signal enables the ROM memory to receive addresses from the address and control-bit registers. After performing an addressing function, Port 0 (BUS) reverts to the input mode and receives the addressed program instruction.

5.91 Software address registers in the microcomputer's resident data memory are used to access data memory and allow for the additional 256 words of external memory provided by RAM memory U10 and U16. Also, output P20 of Port 2 is combined with the address function of Port 0 which extends the data memory space to 512 words. This

512-word memory space includes the 256 RAM locations, leaving 256 locations for external I/O functions. External I/O is treated as part of data memory, with address bit PB7 (P20 of Port 2) used to distinguish memory addresses from external I/O addresses.

5.92 External data memory is accessed with bits PB0 through PB8 and read/write signals. The ALE signal is used to latch PB8 from P20 of Port 2 into the control-bit register (U14) and $\overline{\text{ALE}}$ latches PB0 through PB7 into the address registers (U15, U19, and U20). The $\overline{\text{ALE}}$ is also used to clock inputs of the read/write control (U6, U11).

5.93 The address registers send only address bits PB0 through PB6 to the RAM memory. The eighth ROM memory address bit is completed by the control-bit register which controls PB8. The logic state of PB8 determines which RAM memory locations (080 to 0FF hex and 180 to 1FF hex) are addressed. The remaining bit PB7 is set low to steer the read/write function signal through the read/write control to ROM memory.

5.94 External I/O is addressed when PB7 is set high. With PB7 set high, the read/write control steers the read/write function to I/O data circuits. The read-data function ($\overline{\text{RDD}}$) is steered only to the two data registers (MPW and FPS data registers) located on the microprocessor board; and the write-data function ($\overline{\text{WRD}}$) is sent off-board to Display Assembly A18.

5.95 An external I/O address is sent via the address/data bus $\overline{\text{PB0-PB7}}$ of Microprocessor A11. The output bus of Microprocessor A11 is obtained by inverting the logic states output from Port 0 of the microcomputer. Address bits PB4 and PB5 are used to determine whether the MPW or FPS data register is addressed for a read-data operation. When $\overline{\text{PB4}}$ and $\overline{\text{PB5}}$ are both logic high (PB4 and PB5 both low, or 0), the FPS data register is addressed (addresses 0X or 4X hex, with X = don't care). When $\overline{\text{PB4}}$, or $\overline{\text{PB5}}$, or both are low (PB4, or PB5, or both high), the MPW register is addressed (addresses 1X through 3X hex, and 5X through 7X hex).

5.96 DISPLAY ASSEMBLY A18

5.97 Display Assembly A18 provides the means to comprehensively display signaling information which is provided and controlled by Microprocessor A11. The display assembly consists of two separate boards, Display Driver A17 and Display Board A16. The display driver board interfaces the microprocessor board with the display board.

5.98 The display assembly uses a 16-digit signaling display and three LED displays grouped as follows:

1. signaling display,
2. frequency display,
3. code display, and
4. signal display.

5.99 The signaling display consists of 16 7-segment digit chips (U3 through U18) which show the dialed digits and backward signaling monitored on a call.

5.100 The frequency display is a set of eight LED lamps (700/697, 900/770, 1100/852, 1300/941, 1500/1209, 1700/1336, 1477, and 1633 Hz). These lamps show the frequency content of an MF or DTMF signal.

5.101 The code display uses five LED lamps (KP, ST, STP, ST2P, and ST3P) to display special MF signal codes.

5.102 Seven LED lamps (OFF HOOK, MF, E, M, LOOP, DTMF, and MEMORY) make up the signal display used to identify the type of seizure and signaling mode.

5.103 The above four display groups are located on the display board. Digit selection and the LED segment on/off status of the signaling display, as well as display selection and LED on/off status of the other three displays, are controlled by Microprocessor A11 through interface circuits on the display driver board. In addition to display outputs, the driver board also provides signaling data outputs to CDA Interface A10 (rack-mount Model 2763R), or to External Alarm Relay A10 (portable Model 2763 and Model 2763A).

5.104 The four display groups and external data outputs are treated as a part of the external data-memory space of microcomputer U9 on Microprocessor A11. The microcomputer addresses and writes data to the displays and external outputs via its combined address and data bus and two function-control signals. The function signals, $\overline{ALE}$ and $\overline{WRD}$, control the display driver board circuits which store and decode the address and data bus inputs.

5.105 Display Driver Circuits

5.106 The designated bus bits DB0-DB7 result from inverted bus bits $\overline{PB0-PB7}$ which input the display driver board from Microprocessor A11. Because the bus output of microcomputer U9 is inverted to produce the output bus of the microprocessor board, bus bits DB0-DB7 are logically equivalent to the address/data bit code which outputs directly from the bus port of microcomputer U9 on Microprocessor A11.

5.107 The display driver board uses a common address register and display selector circuit (U13 and U14) to store and decode all display group and data output addressing. The decoded address outputs of the selector circuit are used to switch respective display data through data channels to the display groups or external data outputs.

5.108 The frequency, code, and signal display groups each use a separate data channel. The data channels of the code and signal display are also used to output some data to the CDA interface board, or the external alarm relay driver board.

5.109 The signaling display group is different from the three LED display groups in that it requires two data channels, a digit data channel (U2 and U1) and a segment data channel (U5, U9). The digit and data channels must be addressed separately, and both are controlled by display clear control U4.

5.110 In addition to decoded address outputs to the four display groups and related external data outputs, address register and display selector (U13 and U14) also provide two decoded address outputs used by the CDA interface board to output ASCII and HEX data for use by external equipment.

5.111 Table 5—1 defines the address codes and data bits used to access the four display groups and external data control circuits. Table 5—2 defines in greater detail the hexadecimal or data bit code needed to produce a digit's symbol display for a particular signaling code. The associated LED segment for each data bit is also shown near the bottom of the table. Included are the segment positions of a digit chip. (Notice that a 7-segment digit actually contains eight LEDs. The dp LED is not used, i.e., bit DB7 is always low, or 0.) Bit DB7 is logically equivalent to PB7 which microcomputer U9 must set low to write data to the displays.

5.112 LED Display Operation

5.113 A frequency, code, signal, ASCII, or HEX group address (hexadecimal code 10, 20, 30, 40, or 50 respectively) is latched in address register U13 on the trailing (rising) edge of $\overline{ALE}$. The specific group address is determined by bits DB4 through DB6, with DB0-DB3 and DB7 all set low. Display selector U14 decodes the stored address shortly after the leading (falling) edge of the $\overline{WRD}$ pulse. The decoded address appears as a low on only one of the display selector outputs. The output is held low until the trailing (rising) edge of the $\overline{WRD}$ pulse. Display data appears on the bus during the $\overline{WRD}$ pulse, and the low output of display selector U14 is forced high by the trailing edge of $\overline{WRD}$. This action latches the display data in the appropriate frequency, code, signal, ASCII, or HEX data register. Data stored

in the frequency, code, or signal data register is sent directly to the group LEDs on the display board, and controls which LEDs are turned on. A high data bit input to the data register causes its associated LED to turn on, a low input causes the LED to turn off. The code and signaling data registers also output information for use by external equipment.

5.114 Signaling Display Operations

5.115 The 16-digit display is multiplexed at a rate of 62 Hz, which means all 16 digit chips must be refreshed during a 16-msec time period. Microcomputer U9 on Microprocessor A11 receives an interrupt signal every 1-msec period, and during this period a single digit is refreshed. To refresh a digit, two $\overline{ALE}$ and $\overline{WRD}$ function cycles are required. During the first cycle, the digit register is addressed (hexadecimal code 60), and digit select data is stored in the same manner as is done for the LED lamp display groups. However, the output of the digit register is not sent directly upon latch to the display board. Instead, this data appears at the input of digit selector U1 and remains there until the segment

register is addressed and written to during the second $\overline{ALE}$ and $\overline{WRD}$ cycle. When the segment register is addressed and the group selector (U14) output line to the register goes low (on leading edge of $\overline{WRD}$ pulse), display clear control U4 is triggered. Control U4 is a one-shot which outputs a high signal pulse to the segment register, and a low signal pulse to the digit selector. Both signal pulses are approximately 0.75 msec in duration. During the low pulse period, digit select U1 decodes the latched data of digit register U2, and outputs the required digit enable code to the display board. Also during this period, the high pulse signal enables the segment register which latches segment display data on the trailing edge of the $\overline{WRD}$ pulse. The stored segment data is then sent to the display board. On the display board, the digit selector (U1) output is applied through a digit driver to enable the selected digit chip. The segment data is also applied through signal drivers to the enabled digit chip. At the end of one-shot U1's time period, both the segment register and digit selector outputs are disabled to protect the 16-digit display chips from possible burn-out. (The digit chip blank-out period is not noticeable to an operator viewing the 16-digit display.)

Table 5—1. Display Address/Data Select Codes.

ADDRESS	DATA BITS								DESCRIPTION
	7	6	5	4	3	2	1	0	
10								X	700/697 (CR1)
							X		900/770 (CR2)
						X			1100/852 (CR3)
					X				1300/941 (CR4)
				X					1500/1209 (CR5)
			X						1700/1336 (CR6)
		X							1477 (CR7)
	X								1633 (CR8)
20								X	ST3P (CR20)
							X		ST2P (CR19)
						X			STP (CR18)
					X				ST (CR17)
				X					KP (CR16)
			0						Sets ERROR ALARM input signal to alarm control circuit on CDA Interface/External Alarm Relay Driver A10.
		X							Not used
	1								Sets $\overline{DIGIT\ PRESENT}$ trigger signal to one-shot U11 (DP pulse generator) on CDA Interface A10.

Table 5—1. (Cont'd.)

ADDRESS	DATA BITS								DESCRIPTION
	7	6	5	4	3	2	1	0	
30								X	MEMORY (CR15)
							X		DTMF (CR14)
						X			LOOP (CR13)
					X				MF (CR10)
				X					M (CR12)
			X						E (CR11)
		X							OFF HOOK (CR9)
	1								Sets EXT LINE REV signal input to CDA Interface A10, output at accessory connector J23 is a high LINE REV signal.
40	ALL								Determines the ASCII data code output at accessory connector J23.
50	ALL								Determines the HEX data code output at accessory connector J23.
60					0	0	0	0	Digit 1 (U3)
					0	0	0	1	Digit 2 (U4)
					0	0	1	0	Digit 3 (U5)
					0	0	1	1	Digit 4 (U6)
					0	1	0	0	Digit 5 (U7)
					0	1	0	1	Digit 6 (U8)
					0	1	1	0	Digit 7 (U9)
					0	1	1	1	Digit 8 (U10)
					1	0	0	0	Digit 9 (U11)
					1	0	0	1	Digit 10 (U12)
					1	0	1	0	Digit 11 (U13)
					1	0	1	1	Digit 12 (U14)
					1	1	0	0	Digit 13 (U15)
					1	1	0	1	Digit 14 (U16)
					1	1	1	0	Digit 15 (U17)
					1	1	1	1	Digit 16 (U18)
70								X	LED g
								X	LED f
							X		LED e
					X				LED d
				X					LED c
			X						LED b
		X							LED a
	X								LED dp

Enables respective digit of the signaling display.

Sets on/off status of a digit's LED segment.*
NOTE: See Table 5—2 for specific signaling code displays.

*When X = 1, the LED lamp is turned on.

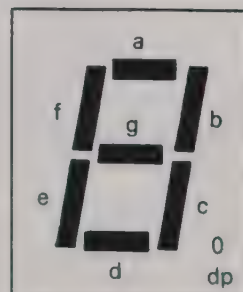
Table 5-2. Digit Display Data Codes.

SIGNALING CODES	DISPLAYED SYMBOLS	HEXADECIMAL DATA CODE	DATA BITS							
			7	6	5	4	3	2	1	0
1	1	30	0	0	1	1	0	0	0	0
2	2	6D	0	1	1	0	1	1	0	1
3	3	79	0	1	1	1	1	0	0	1
4	4	33	0	0	1	1	0	0	1	1
5	5	5B	0	1	0	1	1	0	1	1
6	6	5F	0	1	0	1	1	1	1	1
7	7	70	0	1	1	1	0	0	0	0
8	8	7F	0	1	1	1	1	1	1	1
9	9	73	0	1	1	1	0	0	1	1
0	0	7E	0	1	1	1	1	1	1	0
.	-	01	0	0	0	0	0	0	0	1
#	#	37	0	0	1	1	0	1	1	1
A/ST	a	7D	0	1	1	1	1	1	0	1
B/STP	b	1F	0	0	0	1	1	1	1	1
C/ST2P	c	0D	0	0	0	0	1	1	0	1
D/ST3P	d	3D	0	0	1	1	1	1	0	1
KP	E	4E	0	1	0	0	1	1	1	0
LINE REVERSAL	Q	1D	0	0	0	1	1	1	0	1
WINK	w	1C	0	0	0	1	1	1	0	0
TRANSITION	i	04	0	0	0	0	1	0	0	0
ERROR	E	4F	0	1	0	0	1	1	1	1

NOTE: 1. Codes *, #, A, B, C, and D are DTMF signaling codes.
2. Codes ST, STP, ST3P, and KP are MF signaling codes.

DATA BITS	7	6	5	4	3	2	1	0
7-SEGMENT LEDs	dp	a	b	c	d	e	f	g

LED POSITIONS
FOR 7-SEGMENT
DIGIT DISPLAYS
U3 THROUGH U18



5.116 CDA INTERFACE/EXTERNAL ALARM RELAY DRIVER A10

5.117 The CDA interface board is used only with rack-mount Model 2763R. Its function is to provide monitored signaling information for use by auxiliary equipment such as a Model 2765A Call Disposition Analyzer, printer, or computer. The output signaling data is interfaced through Accessory Board A12 to connector J23 at the rear of the Model 2763R. Jack J23 connects directly to auxiliary equipment and outputs information concerning dialed digits (MF, DTMF, or DP), MF codes, and loop or E&M supervision. Two control line outputs as well as a reset input are also provided at J23.

5.118 In addition to the data sent to J23, the CDA interface outputs an alarm contact closure when the front-panel ERROR FUNCTION switch is enabled and the 2763R detects an error in monitored signaling. External Alarm Relay Driver A10, which replaces CDA Interface A10 in the Model 2763 and Model 2763A, also provides the alarm contact closure. This contact closure is the only output of the external alarm relay driver board. The alarm output of either board is a tip-to-ring closure which outputs at the front-panel ERROR ALARM phone jack.

5.119 The CDA interface circuits are grouped as follows:

1. ASCII and HEX data channels,
2. code and signal data channels,
3. control outputs and reset input, and
4. error alarm circuit.

5.120 ASCII and HEX Data Channels

5.121 The ASCII and HEX data channels each contain a data register which is addressed and written to in the same manner as the LED display channels on Display Driver Board A17. The required addresses (hexadecimal 40 for the ASCII channel, and 50 for the HEX channel) are stored and decoded by address register and display selector circuits U13 and U14 on the display driver board. The ASCII and HEX data bits are latched in the respective ASCII register (U8 and U9) or HEX register (10) on the rising edge of the $\overline{WRD}$ pulse applied to the display driver board. The data outputs of the registers are inverted (buffers U3, U4, and U5) and then sent to accessory connector J23.

5.122 The ASCII parallel-bit printer information is available when the $\overline{PD}$ (printer data) line at J23 is low.

The ASCII data provides digit and character information, as well as printer operation commands.

5.123 The HEX channel provides digit and signaling error information for use by a Model 2765A Call Disposition Analyzer. This HEX coded information is available when the $\overline{DP}$ (data present) line goes low.

5.124 Code and Signal Data Channel

5.125 The code and signal data are also presented for use by a Model 2765A Call Disposition Analyzer. This data originates from the code and signal registers (U6, U7, U10, and U12) on the display driver board and is in agreement with the respective LED displays, but is independent of the $\overline{DP}$ line status. The MF code channel inputs (EXT KP, and EXT ST through ST3P) are inverted (buffers U1 and U2A) before output as $\overline{KP}$ and $\overline{ST}$ through $\overline{ST3P}$. Signal channel inputs (EXT OFF HOOK, and EXT E and M) are inverted twice (buffers U7A-B and U2B-D) before output as OFF HOOK, and E and M signals. Input $\overline{EXT LINE REV}$ is inverted once (buffer U6A), and appears as output LINE REV.

5.126 Control Outputs and Reset Input

5.127 The two data control outputs are the $\overline{PD}$ and $\overline{DP}$ signals. The $\overline{PD}$ output originates directly from the $\overline{PRINTER DATA}$ input received from Microprocessor A12, and signals the availability of ASCII-coded data. The $\overline{DP}$ (DATA PRESENT) output is a 0.1-msec pulse used to signal the availability of HEX coded data. The $\overline{DP}$ pulse is produced when the $\overline{DIGIT PRESENT}$ input goes low, triggering one-shot U11. Although the digit present line is accessed with the same address (hexadecimal 20) as the LED code display, the data on the line does not affect the state of the LEDs.

5.128 The reset input line allows a Model 2765A Call Disposition Analyzer, or other external equipment, to remotely reset the Model 2763R if the front-panel REMOTE RESET switch is set at IN. This external $\overline{RESET}$ input signal outputs the CDA interface as the $\overline{EXT RES IN}$ signal which is OR-wired with the $\overline{REM RES IN}$ signal line from the front-panel REMOTE RESET IN phone jack J12. The $\overline{RESET}$ is also used independently of the REMOTE RESET switch setting to generate a contact closure (see Main Input Board A4) which outputs the Model 2763R at the REMOTE RESET OUT phone jack J11.

5.129 Error Alarm Circuit

5.130 An error alarm circuit is present on both the CDA interface and the external alarm relay driver board. This circuit consists of an alarm driver (U12 and Q1 for the CDA interface, and U1 and Q1 for the external alarm relay driver board) and an alarm relay (K1 for both boards).

5.131 The ERROR ALARM input to the alarm circuit is accessed with the same address (hexadecimal 20) as the LED code display circuit on the display driver board, but the data on the alarm input does not affect the LED data. With the ERROR FUNCTION switch enabled, a detected signaling error condition results in an ERROR

ALARM signal input to the alarm driver which energizes relay K1. An energized K1 causes a contact closure between ERROR ALARM TIP and ERROR ALARM RING. This contact closure appears at the front-panel ERROR ALARM phone jack J9.

SECTION 6

ALIGNMENT

6.1 This section contains the information needed to align the Model 2763, 2763A, and 2763R Signaling Displays.

6.2 The following paragraphs provide a complete set of adjustment procedures required for alignment of the signaling display. These procedures can be used for periodic maintenance and repair checks. Table 6—1 lists the test equipment required for the alignment procedures presented. Personnel performing these procedures must be familiar with the test equipment recommended. **No adjustments should be made without proper test equipment or qualified personnel.**

6.3 Alignment is presented as a series of adjustment procedures for easy reference. Alignment should be performed in the exact sequence presented as adjustment steps are often dependent on previously performed adjustments. Also, the procedures assume switch and control positions remain as set unless specific instructions require new positions.

CAUTION

Ensure that the POWER switch is placed off when either removing or replacing extenders or boards. Failure to do so can result in damage to the signaling display.

6.4 PREPARATION FOR ALIGNMENT

6.5 Perform the following steps:

1. Shut down the signaling display (POWER switch off), and disconnect the power cord.
2. Perform the instruction procedures presented in paragraph 3.19 (for Models 2763 and 2763A), or paragraph 3.21 (for Model 2763R) to obtain access to the pc boards located inside the card cage.
3. Connect the signaling display power cord.

6.6 ALIGNMENT PROCEDURES**6.7 MAIN INPUT A4 ALIGNMENT****6.8 Preliminary**

1. Place the POWER switch off.
2. Remove Main Input A4 from J4 of the card cage assembly.
3. Insert the extender board into the card cage assembly, and connect Main Input A4 to the extender board.

4. Check for secure connections between the card cage, extender board, and main input board. **Faulty connections can result in erratic operation of the main input board.**

5. Connect the signal generator, frequency counter, and ac voltmeter as shown in Figure 6—1. Ensure that inputs L1 and L2 are connected in parallel.
6. Adjustments for Main Input A4 consist of the L1 and L2 input balance adjustment (R15), and the overall main input gain adjustment (R1).

6.9 Input Balance Adjustment

1. Place the POWER switch on.
2. Set the signal generator for a continuous sinusoidal output of 1,000 Hz at 0 dBm (0.7746 V rms).
3. Refer to Figure 7—13.
4. Connect the ac voltmeter for a reading at TP2.
5. Record the voltage (V rms) reading at TP2 for later use.
6. Connect the ac voltmeter for a reading at TP1.
7. Adjust R15 so that the voltage level at TP1 equals the recorded reading of TP2 ± 0.001 V rms.

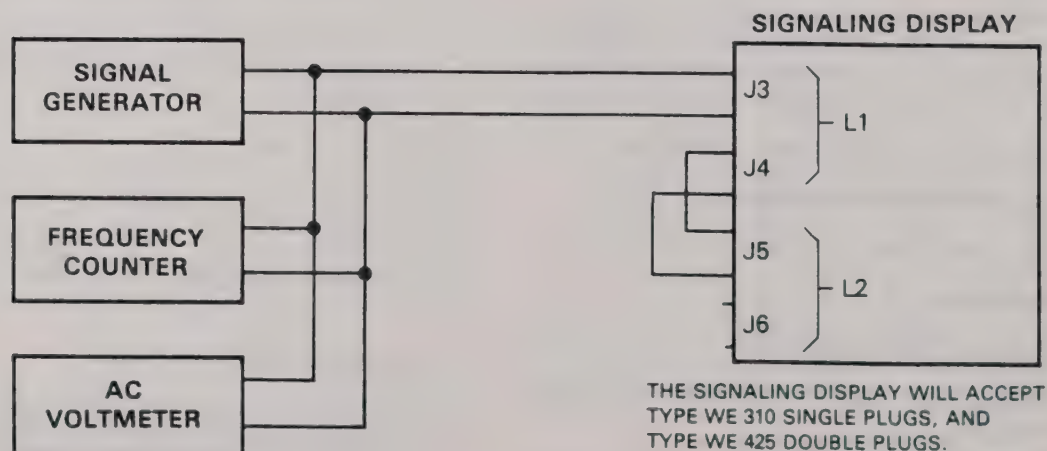
6.10 Gain Adjustment

1. Place the POWER switch on.
2. Set the signal generator for a continuous sinusoidal output of 1,000 Hz at 0 dBm (0.7746 Vrms).
3. Depress and latch the L1 PUSH TO SELECT switch, and check that L2 PUSH TO RELEASE is released, or off.
4. Refer to Figure 7—13.
5. Connect the ac voltmeter to Pin 18 (DTMF SIGNAL output).
6. Adjust R1 for a reading of 2.0 ± 0.01 Vrms at Pin 18.
7. Place the POWER switch off.
8. Disconnect the main input board from the extender board, and remove the extender board from the card cage.
9. Insert Main Input A4 into J4 of the card cage.

Table 6—1. Required Alignment Test Equipment.

ALIGNMENT PROCEDURES	EQUIPMENT	USE
*Main Input A4 and *MF Detectors A5, A7, and A8	Signal Generator with an output referenced to 600 ohms	Supplies continuous sinusoidal signals with a dial accuracy of 1 Hz
	Frequency Counter	Measures audio frequencies with a resolution of 0.1 Hz
*Line Conditioner A3	RMS AC Voltmeter	Measures signal levels referenced to 600 ohms with a resolution of 0.1 dB
	Variac, or Powerstat	Provides a 20-Vrms, 60-Hz signal
	DCV Supply No. 1; (HP6236B, or equivalent)	Provides 0 to + 20-Vdc signal levels
	DCV Supply No. 2; (HP6116A, or equivalent)	Provides 0 to – 40-Vdc signal levels
	Two RCL networks as shown in Figure 6–4	Interfaces external signal sources with the 2763 Signaling Display
Microprocessor A11	Digital DC Voltmeter	Measures dc signal levels with a resolution of 1 mv
	Frequency Counter	Measures audio frequencies with a resolution of 0.1 Hz
	Oscilloscope	Displays a pulse waveform for timing measurements

*A suitable 44-pin dual-edge extender board is needed when aligning a card cage plug-in board to allow access to test points and adjustment potentiometers.



A02591-01

Figure 6—1. Initial Setup for Main Input A4 Alignment.

6.11 MF DETECTOR A5, A7, AND A8 ALIGNMENT

6.12 Preliminary

6.13 Each MF detector board provides two of the six separate filter-detector channels required for MF signaling. Each filter-detector channel contains a narrowband filter which is tuned for its input frequency of interest as shown in Figure 6-2. Each narrowband filter is provided with a center frequency adjust and a bandwidth adjust. To align or tune the signaling display for a selected MF signaling frequency, refer to Table 6-2 which gives the appropriate MF detector board, adjustment potentiometers, and alignment test point for each MF signaling frequency, and proceed as follows.

1. Place the POWER switch off.
2. Remove the MF detector board (A5, A7, or A8) requiring alignment from the card cage.
3. Insert the extender board into the card slot of the removed detector board, and connect the detector board to the extender.
4. Check for secure connections between the card cage, extender, and MF detector board. **Faulty connections can result in erratic operation of the detector board.**
5. Connect the signal generator, frequency counter, and ac voltmeter as shown in Figure 6-3.
6. Latch the L1 PUSH TO SELECT switch.

6.14 MF Narrowband Filter Adjustments

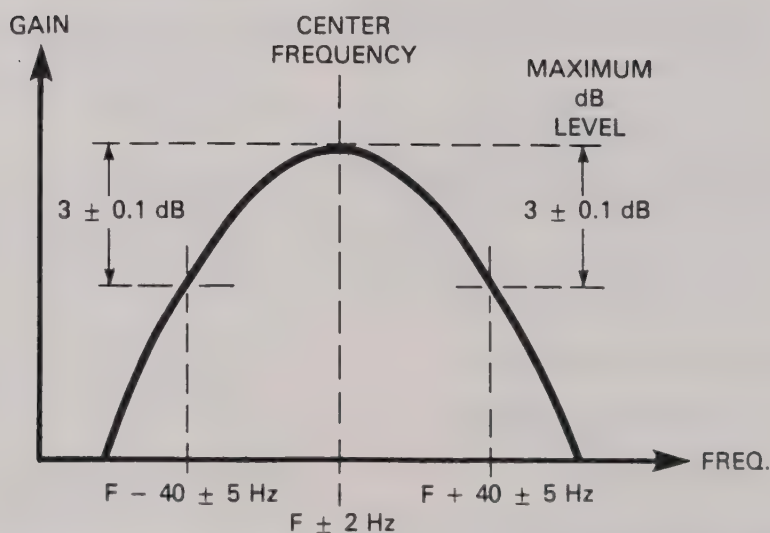
1. Place the POWER switch on.
2. Set the signaling generator for a nominal 0-dB output level, and adjust the generator for a continuous sinusoidal output at the MF signaling frequency of interest (700, 900, 1100, 1300, 1500, or 1700 Hz).
3. Refer to Figure 7-15.
4. Connect the ac voltmeter to the alignment test point (TP1, or TP2) specified in Table 6-2.
5. Adjust the frequency potentiometer (R47, or R64) specified in Table 6-2 for a maximum dB gain as

shown in Figure 6-2. The signal generator output level can be adjusted slightly to allow for a convenient reading of the maximum potentiometer adjustment. Record the maximum dB adjustment. This step completes the center frequency adjustment of the narrowband filter. Continue to step 6 for the bandwidth adjustment.

6. Without changing the signal generator output level, slowly lower the frequency until the dB level at the alignment test point drops 3 ± 0.1 dB below the maximum reading recorded in step 5.
7. The frequency output of the signal generator should read 40 ± 5 Hz lower than the frequency of step 2. Proceed to step 10 if the frequency reading is within limits, otherwise go to step 8.
8. Without changing the signal generator output level, set the frequency 40 ± 5 Hz lower than the frequency of step 2.
9. Adjust the bandwidth potentiometer (R26 or R63) specified in Table 6-2 for a dB reading which is 3 ± 0.1 dB below the recorded maximum reading of step 5.
10. Without changing output level, slowly raise the generator frequency until the dB level at the test point again drops 3 ± 0.1 dB below the recorded reading of step 2.
11. The frequency output of the signal generator should read 40 ± 5 Hz above the frequency of step 2. Proceed to step 15 if the frequency is within limits, otherwise go to step 12.
12. Without changing output level, set the generator frequency 40 ± 5 Hz above the frequency of step 2.
13. Adjust the bandwidth potentiometer for a dB reading at the test point which is 3 ± 0.1 dB below the recorded reading of step 5.
14. Return to step 6, and repeat steps 6 through 14 as necessary.
15. This completes the MF narrowband filter adjustments for a selected MF signaling frequency. Beginning with paragraph 6.12, repeat the entire alignment procedure for each filter-detector channel which requires alignment.

Table 6—2. MF Narrowband Filter Adjustments.

INPUT FREQUENCY	MF DETECTOR BOARD	ADJUSTMENT POTENTIOMETERS		ALIGNMENT TEST POINT
		FREQ. ADJ.	BANDWIDTH ADJ.	
700 Hz	A5	R47	R26	TP1
900 Hz	A5	R64	R63	TP2
1100 Hz	A7	R47	R26	TP1
1300 Hz	A7	R64	R63	TP2
1500 Hz	A8	R47	R26	TP1
1700 Hz	A8	R64	R63	TP2



WHERE F = 700, 900, 1100, 1300, 1500, or 1700-Hz INPUT FREQUENCY

A02589-01

Figure 6—2. MF Narrowband Filter Adjustment.

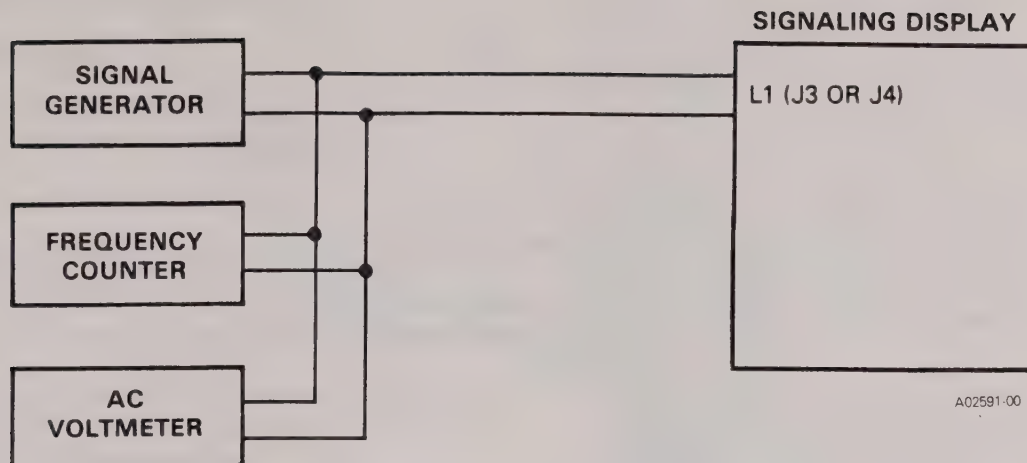
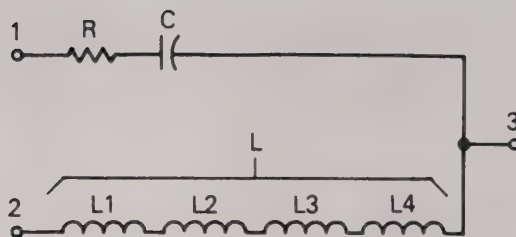


Figure 6-3. Initial Setup for MF Detector A5, A7, or A8 Alignment.

6.15 LINE CONDITIONER A3 ALIGNMENT

6.16 Preliminary

1. Place the POWER switch off.
2. Remove Line Conditioner A3 from J3 of the card cage assembly.
3. Insert the extender board into J3 of the card cage, and connect Line Conditioner A3 to the extender board.
4. Check for secure connections between the card cage, extender board, and line conditioner board.
Faulty connections can result in erratic operation of the line conditioner board.
5. Prepare two identical assemblies of the RCL network shown in Figure 6-4. The 32-mH inductive load for each network can be obtained with four series hold coils (L1, L2, L3, and L4) of 8 mH each.
6. Connect the variac, two dc supplies, and two RCL networks as shown in Figure 6-5. Ensure that ground lug J2 is connected to the common jacks of the variac and dc supplies.
7. Adjustments for Line Conditioner A3 consist of the L1 and L2 input threshold adjustment (R2), and 60-Hz reject circuit adjustments (R43 and R44). Prior to the input threshold and reject circuit adjustments, the three potentiometers (R2, R43, and R44) are preset to designated levels specified in steps 8 through 15 which follow.
8. Place the signaling display POWER switch to on. The power switches of the variac and power supplies remain off at this time.
9. Refer to Figure 7-11.
10. Connect the dc voltmeter between TP1 and ground lug J2.
11. Set R2 fully counterclockwise for approximately -12 V dc at TP1.
12. Connect the dc voltmeter between TP2 and ground lug J2.
13. Adjust R44 for a $-4.7 \pm 0.2\text{ V dc}$ indication at TP2.
14. Connect the dc voltmeter between TP3 and ground lug J2.
15. Adjust R43 for a $+4.7 \pm 0.2\text{ V dc}$ indication at TP3.
16. This completes the preliminary settings for potentiometers R2, R43, and R44 which will be used for the input threshold and 60-Hz reject circuit adjustments.

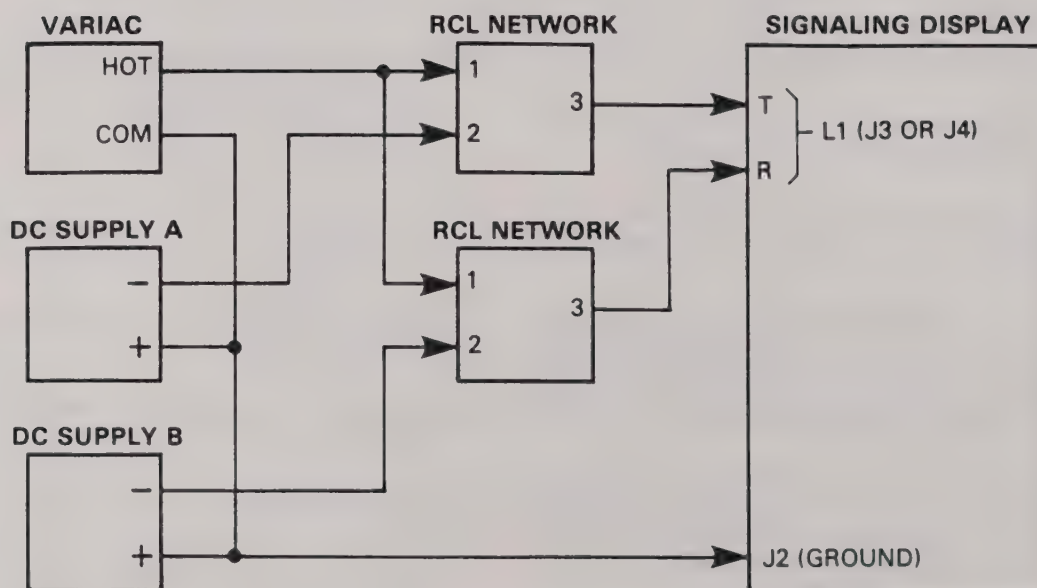


NOTE: L1, L2, L3, L4 ARE HOLD COILS
(NE PART NUMBER 4502-00-200, OR
EQUIVALENT).

$R = 200 \Omega$
 $C = 2.0 \mu F$
 $L = 32 \text{ mH}$
 $L1 = L2 = L3 = L4 = 8 \text{ mH}$

A02590-01

Figure 6-4. RCL Network for Line Conditioner
A3 Alignment.



THE SIGNALING DISPLAY WILL ACCEPT
TYPE WE 310 SINGLE PLUGS, AND
TYPE WE 425 DOUBLE PLUGS.

A02589-00

Figure 6-5. Initial Setup for Line Conditioner A3 Alignment.

6.17 Input Threshold Adjustment

1. Refer to Figure 7–11.
2. Connect the dc voltmeter between TP4 and ground lug J2 to monitor the L1 tip lead input level.
3. Set dc supply A for a -5.5 ± 0.1 V dc input at TP4.
4. Connect the dc voltmeter between TP5 and ground lug J2 to monitor the L1 ring lead input level.
5. Set dc supply B for a -35 ± 0.5 V dc input at TP5.
6. If the signaling display's OFF HOOK lamp is off, adjust R2 clockwise until the lamp turns on to indicate an off-hook condition.
7. With the OFF HOOK lamp on, slowly adjust R2 counterclockwise until the lamp just changes from on to off, indicating an on-hook condition.
8. This completes the input threshold adjustment for both the L1 and L2 input ports. Without disturbing the dc supply inputs and the on-hook (lamp off) indication, continue to the 60-Hz reject adjustment procedure of paragraph 6.18.

6.18 60-Hz Reject Adjustment

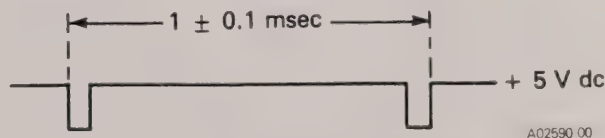
1. Complete the preliminary (paragraph 6.16) and input threshold (paragraph 6.17) adjustments. Ensure that the -5.5 ± 0.1 V dc (TP4) and -35 ± 0.5 V dc inputs are still present to simulate an off-hook input condition.
2. Connect the ac voltmeter between TP4 and ground lug J2.
3. Set the variac for a 20 ± 0.5 Vrms indication at TP4. This step places a 60-Hz signal onto the dc levels of the L1 tip and ring inputs.
4. The OFF HOOK lamp should be off (on-hook indication) at this time. Go to step 6 if the lamp is off, otherwise go to step 5.
5. Without changing the variac's output level, disconnect the variac input to the RCL networks. Slowly adjust R44 counterclockwise until the OFF HOOK lamp changes from on to off, then reconnect the variac input to the RCL network. Repeat step 5 until the lamp remains off after the variac input is reconnected.
6. Slowly adjust R44 clockwise until the OFF HOOK lamp changes from off to on, indicating an off-hook condition.

7. Connect the dc voltmeter between TP4 and ground lug J2.
8. Set dc supply A so that the dc level at TP4 changes from -5.5 ± 0.1 to -5.1 ± 0.01 V dc.
9. Slowly adjust R43 counterclockwise until the OFF HOOK lamp just changes from on to off, indicating an on-hook condition. The lamp may flicker on and off for a short period of time. If the lamp continues to flicker, further adjust R43 slowly counterclockwise until the lamp remains off after a short period of time.
10. Place the POWER switch off. The line conditioner board adjustments are completed. Remove the extender board and reinsert Line Conditioner A3 into J3 of the card cage.

6.19 MICROPROCESSOR A11 ALIGNMENT

6.20 Alignment of Microprocessor A11 requires only setting the pulse repetition rate of the interrupt generator circuit. Timing adjust R7 provides the control for this adjustment as follows:

1. Place the POWER switch off.
2. Remove the protective shield covering the microprocessor board.
3. Place the POWER switch on.
4. Refer to Figure 7–25.
5. Connect the oscilloscope to Pin 8 (interrupt monitor) of P2 for a display of the generated interrupts as shown in Figure 6–6.
6. Adjust potentiometer R7 for a 1 ± 0.1 msec time period between the generated interrupt pulses.
7. Place the POWER switch off and remove the oscilloscope.
8. Replace the protective shield.



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Figure 6–6. Interrupt Timing Adjustment.

SECTION 7**DIAGRAMS**

7.1 This section contains diagrams which document the circuit assemblies within the Model 2763, 2763A, and 2763R Signaling Displays. The diagrams consist of the following:

1. System block diagrams,
2. System functional diagrams,
3. Parts location diagrams, and
4. Schematic diagrams.

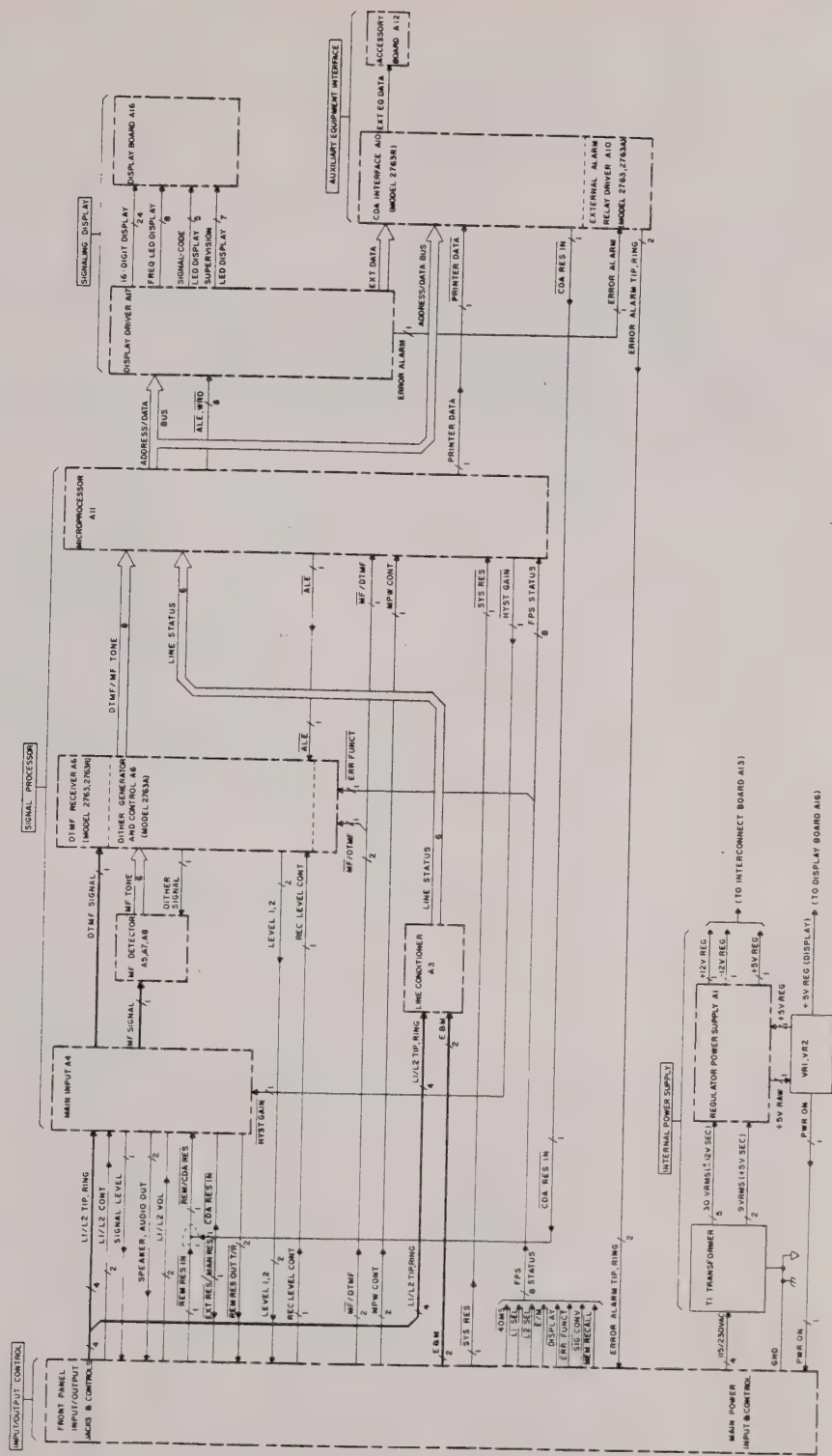


Figure 7-1. System Block Diagram.

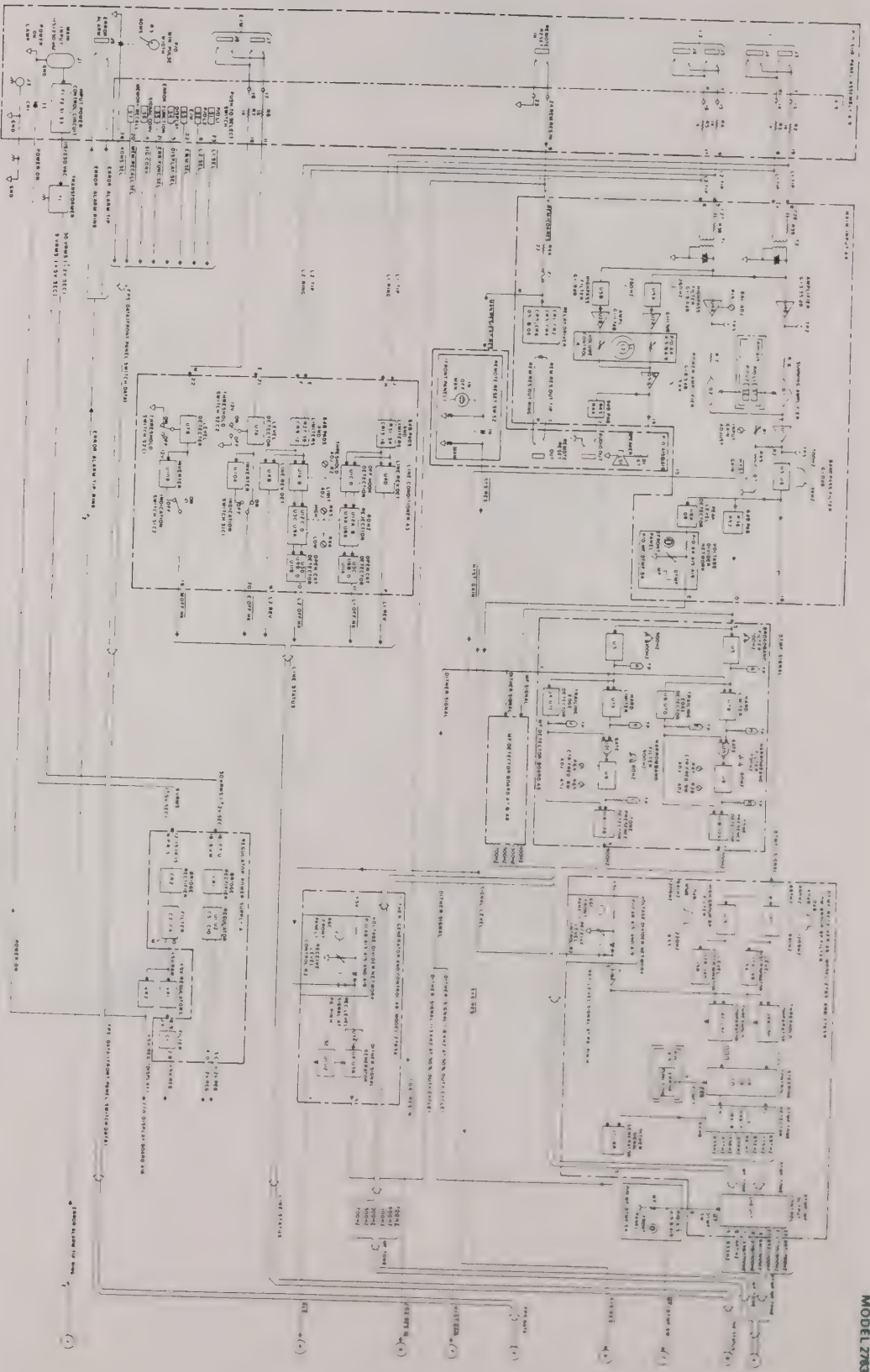


Figure 7-2. System Functional Diagram.
(Sheet 1 of 2)

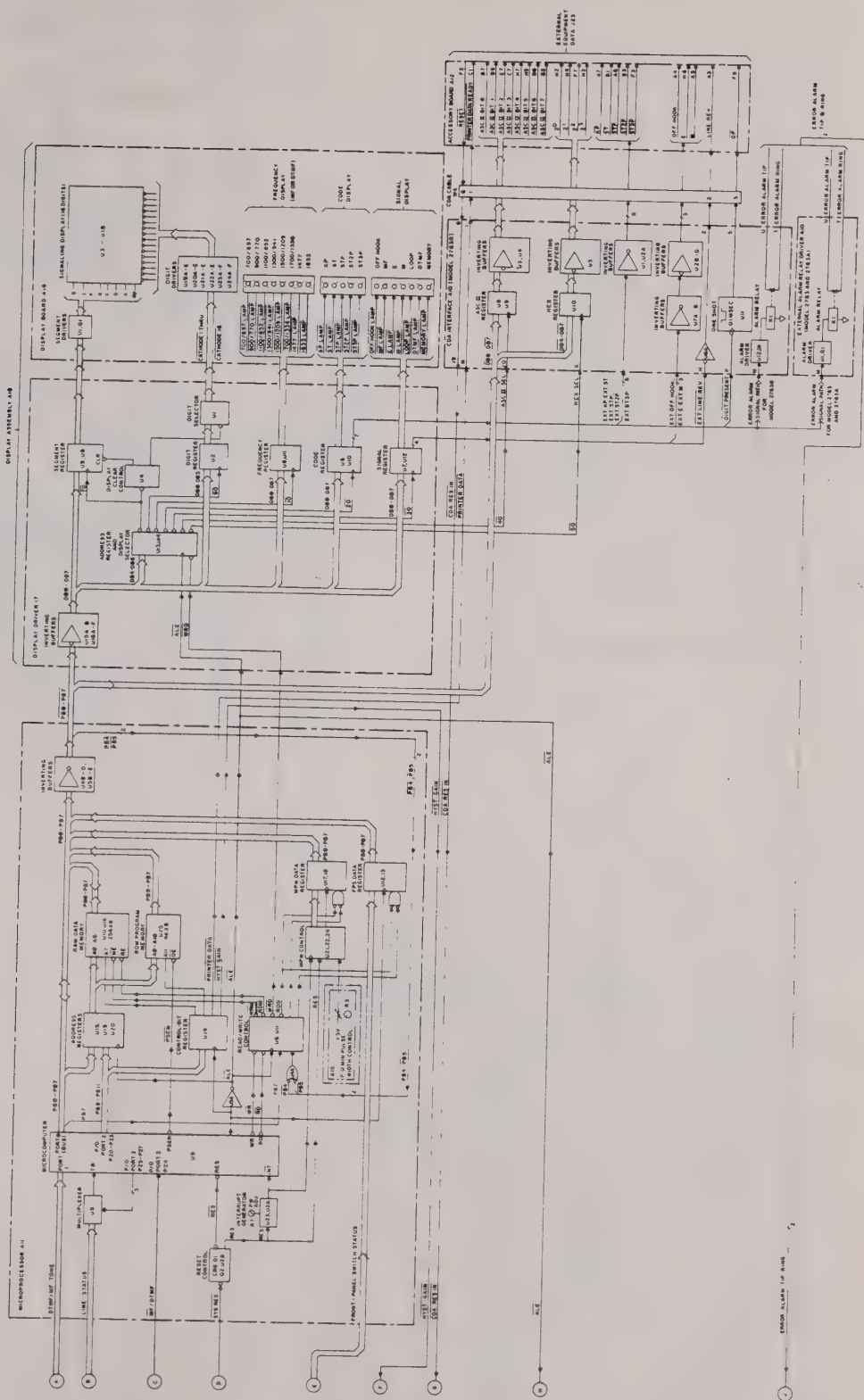


Figure 7-2. System Functional Diagram.
(Sheet 2 of 2)

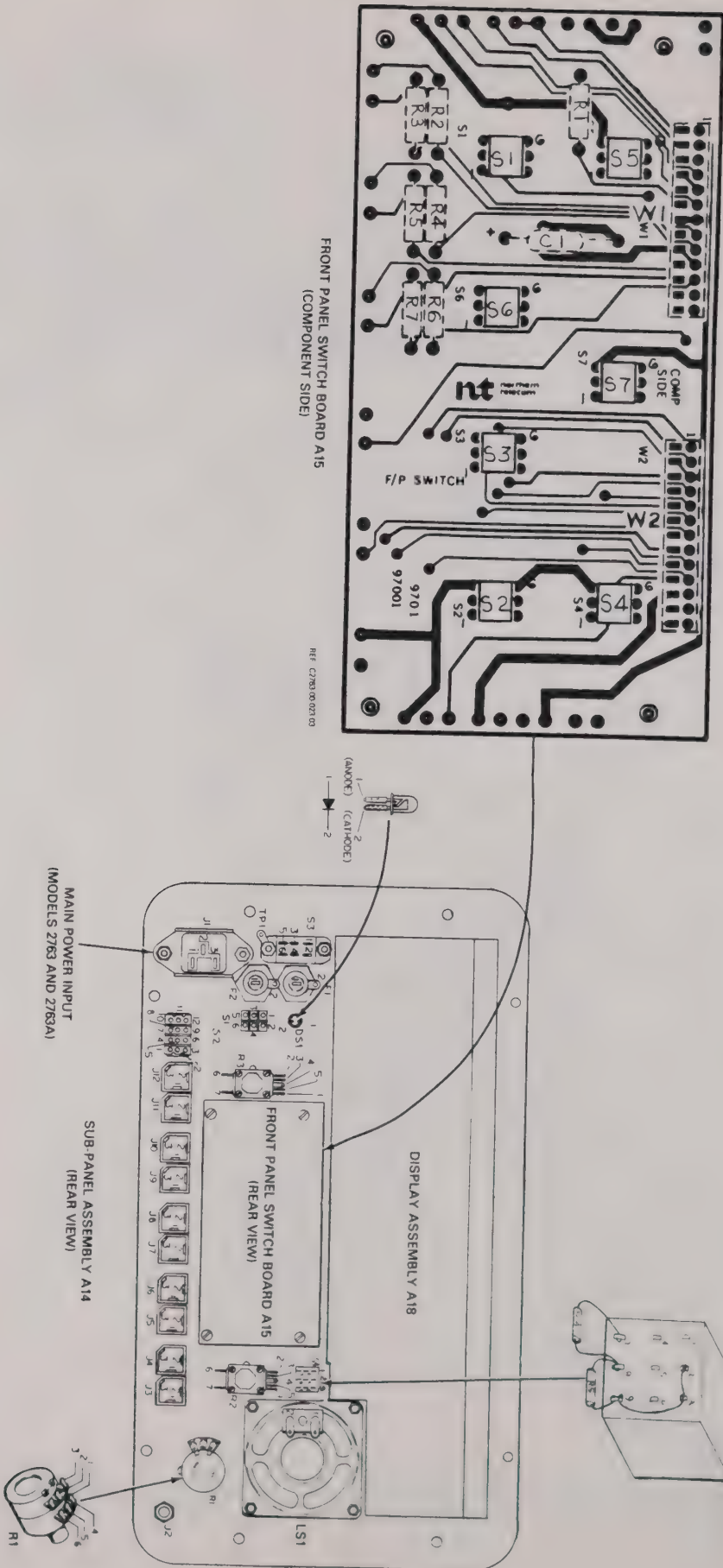
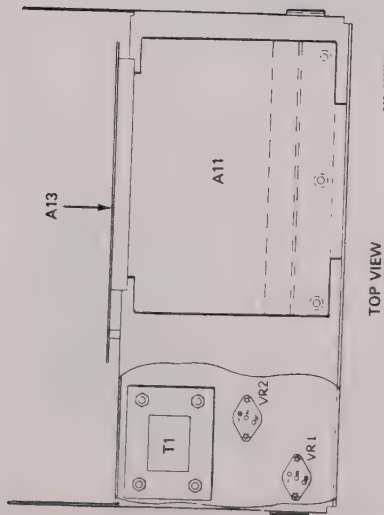


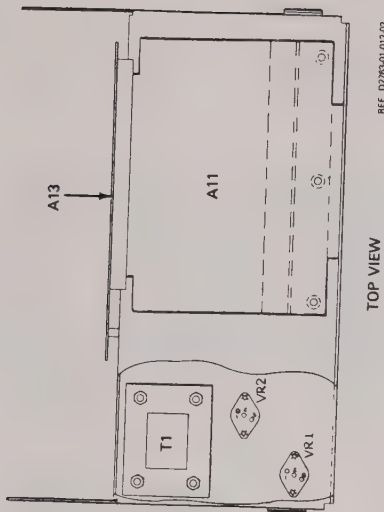
Figure 7-3. Overall Assembly Parts Location Diagram. (Sheet 1 of 2)

MODEL 2763/2763A
CARD CAGE ASSEMBLY A14

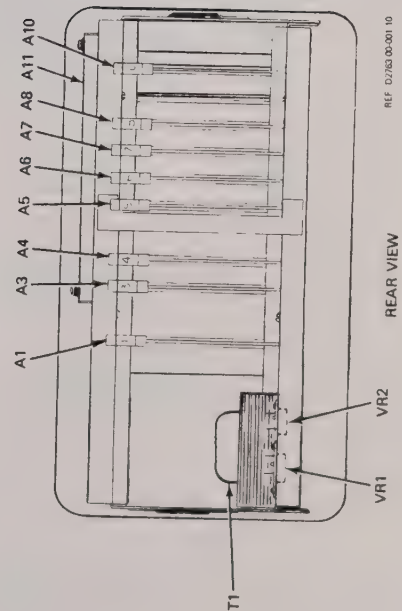


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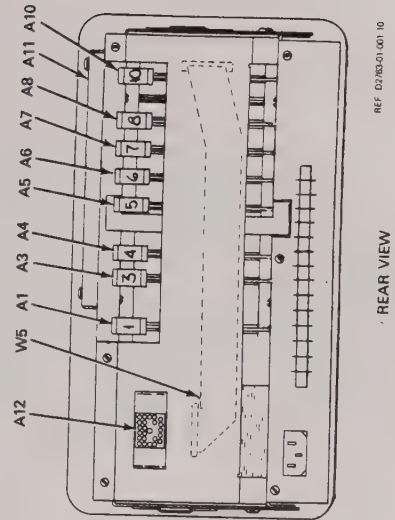
MODEL 2763R
CARD CAGE ASSEMBLY A14



REF. D2763-01-012-02

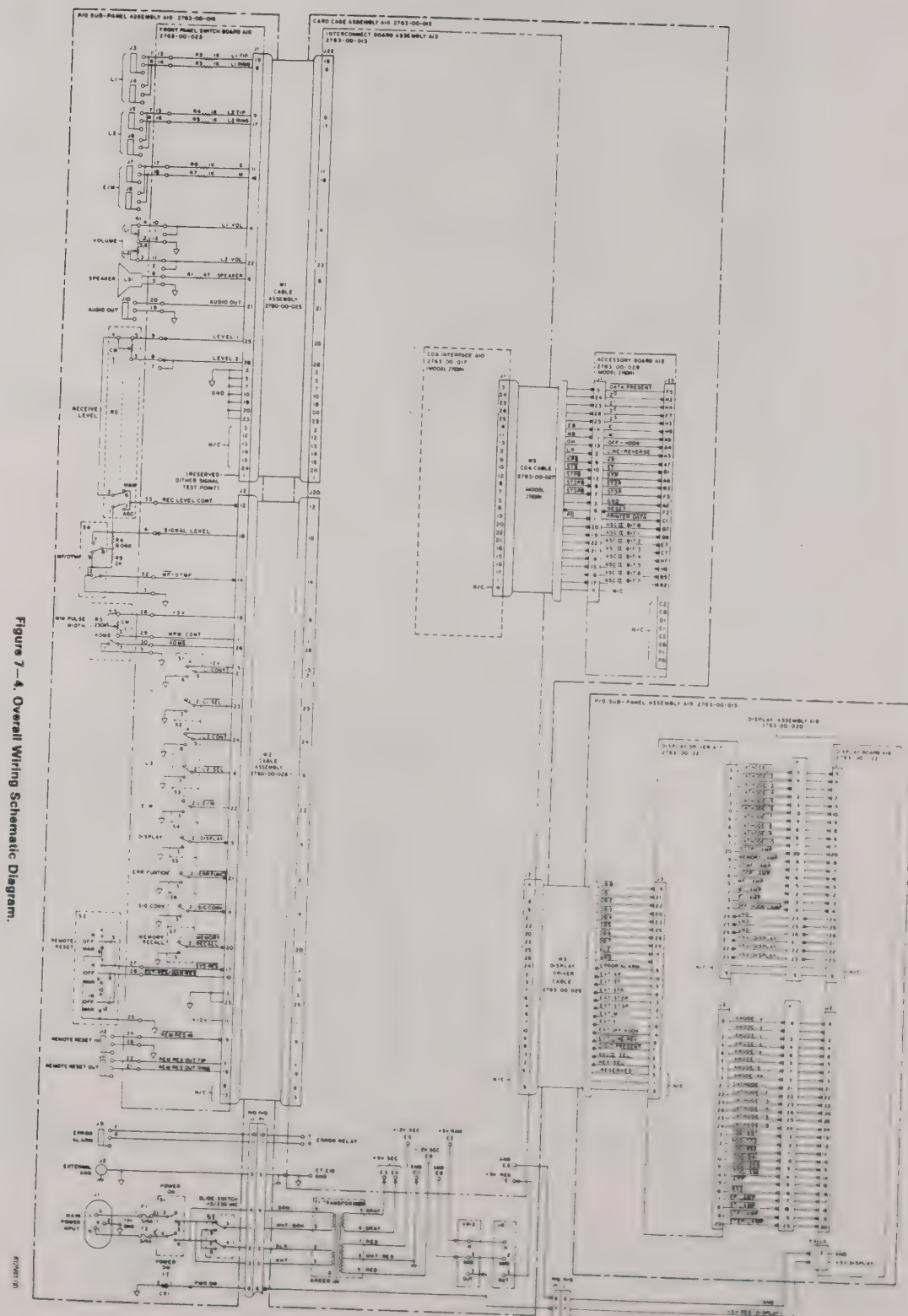


REF. D2763-00-001-10



REF. D2763-01-001-10

Figure 7-3. Overall Assembly Parts Location Diagram. (Sheet 2 of 2)



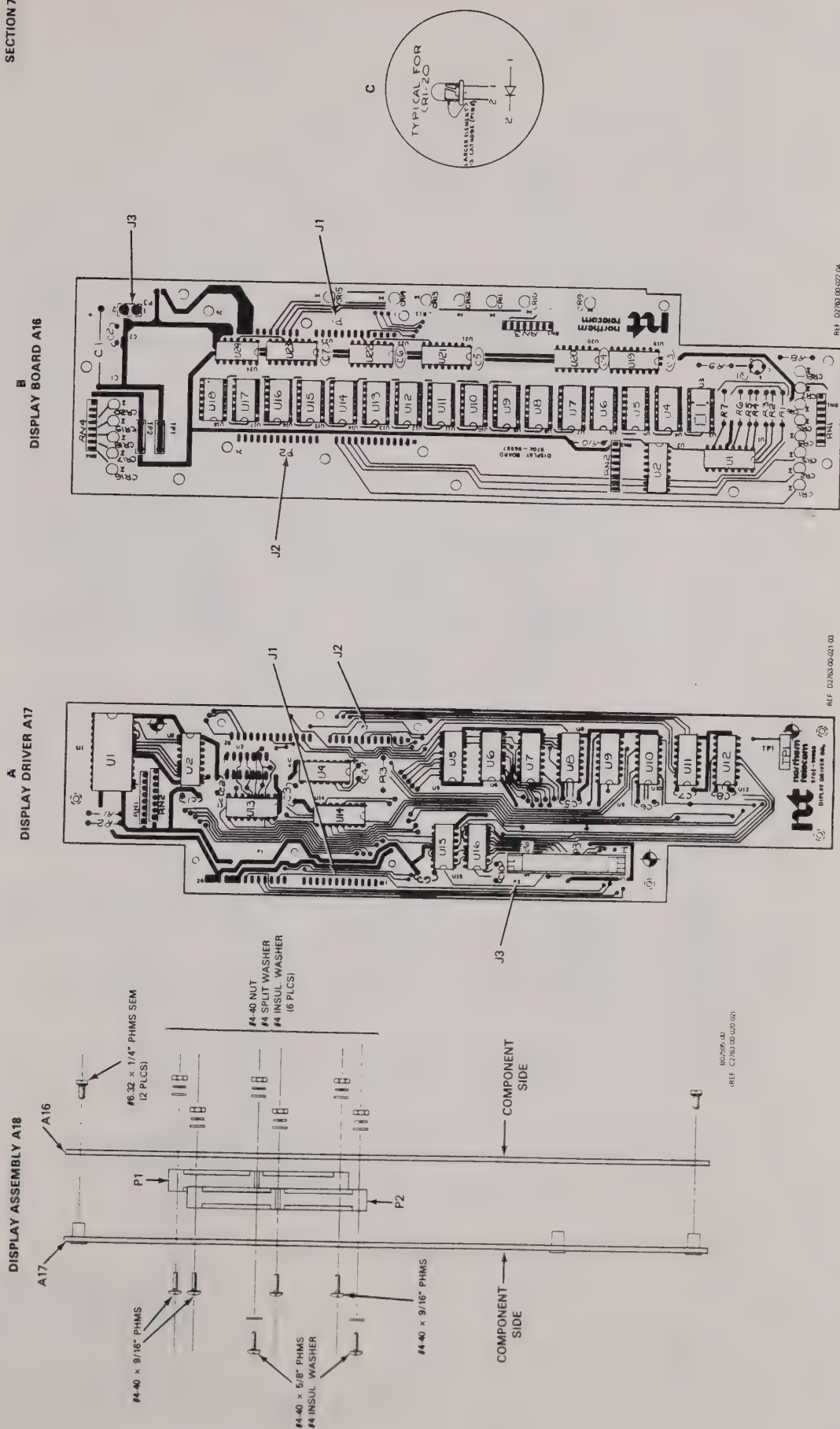
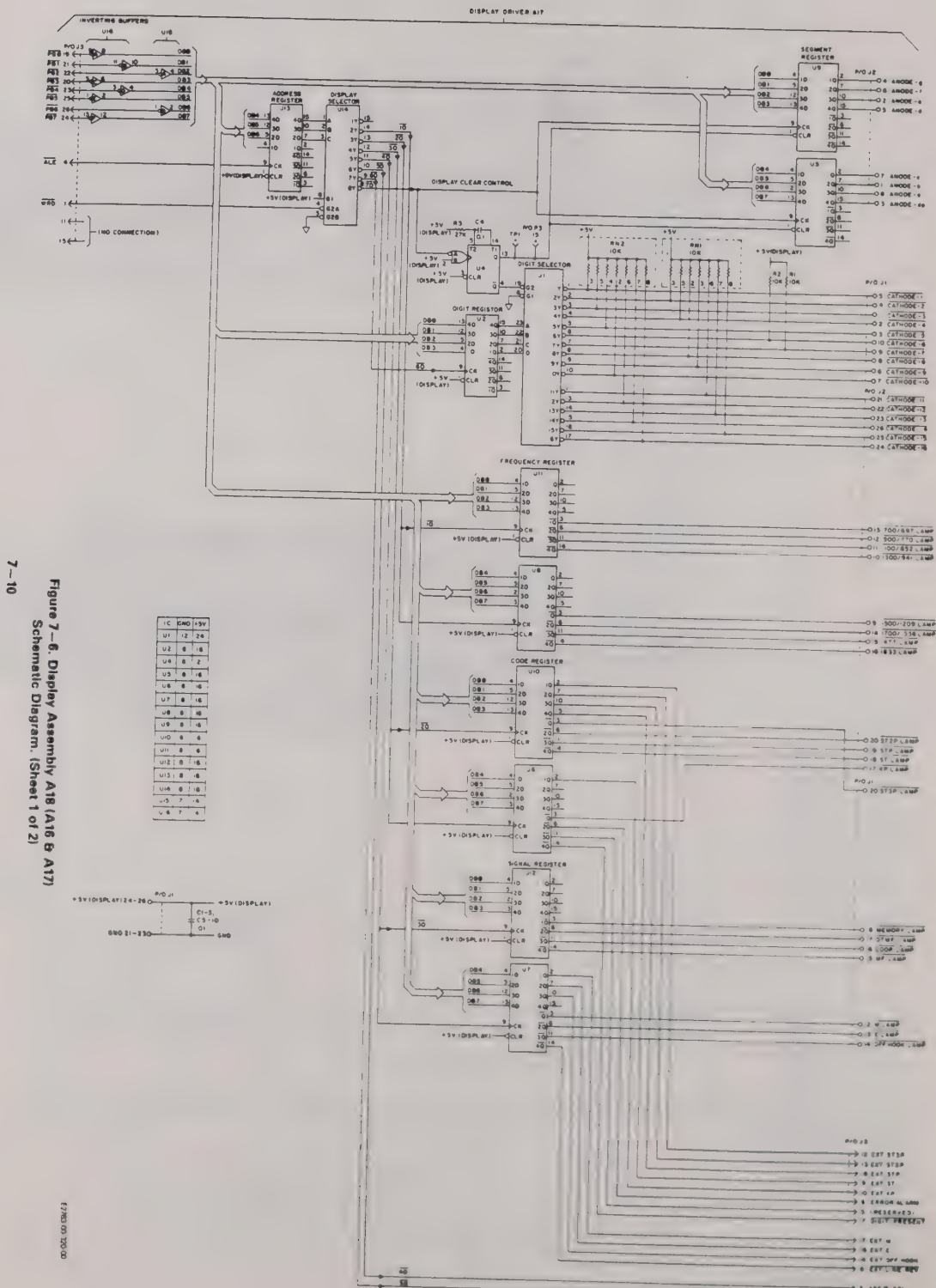


**Figure 7-5. Display Assembly A18 (A16 & A17)
Parts Location Diagram.**



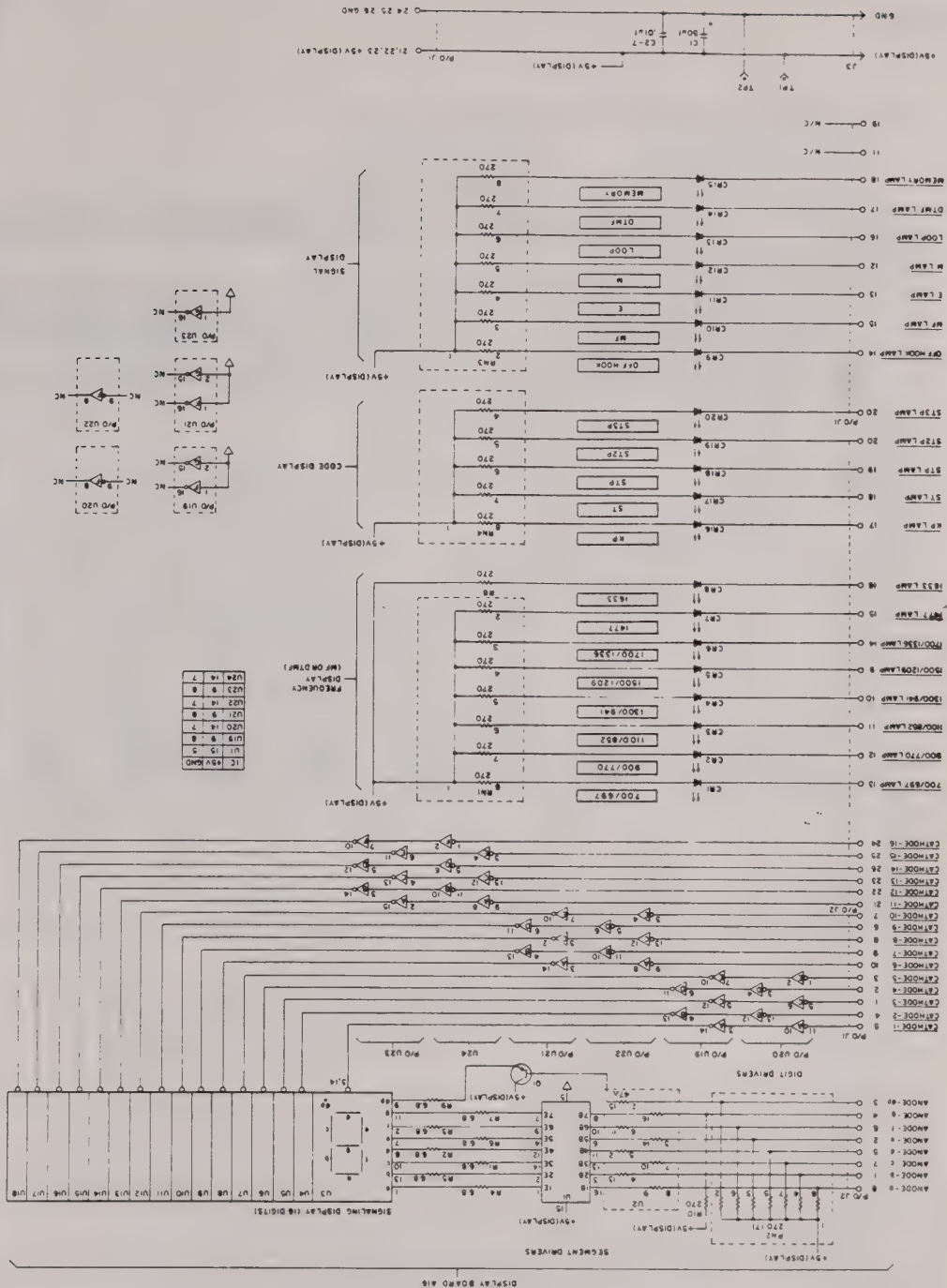
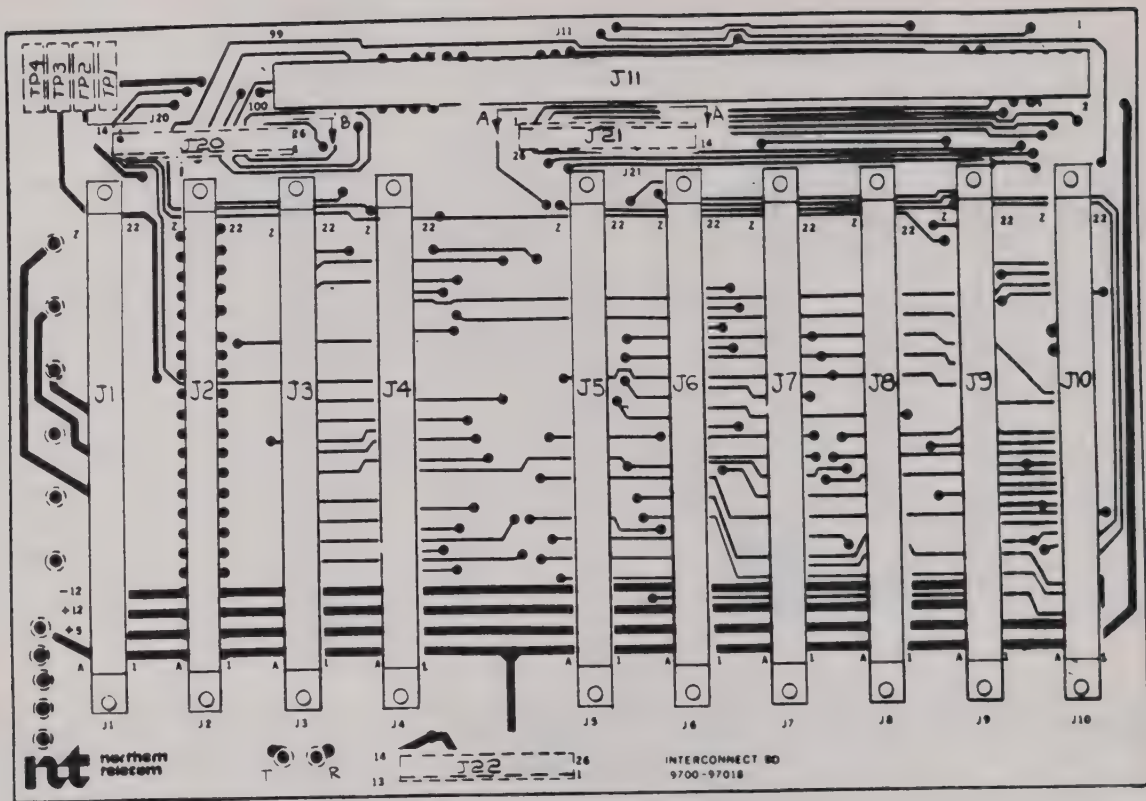


Figure 7-6. Display Assembly A18 (A16 & A17)
Schematic Diagram. (Sheet 2 of 2)



D2763-00-013-08

Figure 7-7. Interconnect A13 Parts Location Diagram.



7-13



Figure 7-8. Interconnect A13 Schematic Diagram.
(Sheet 2 of 2)

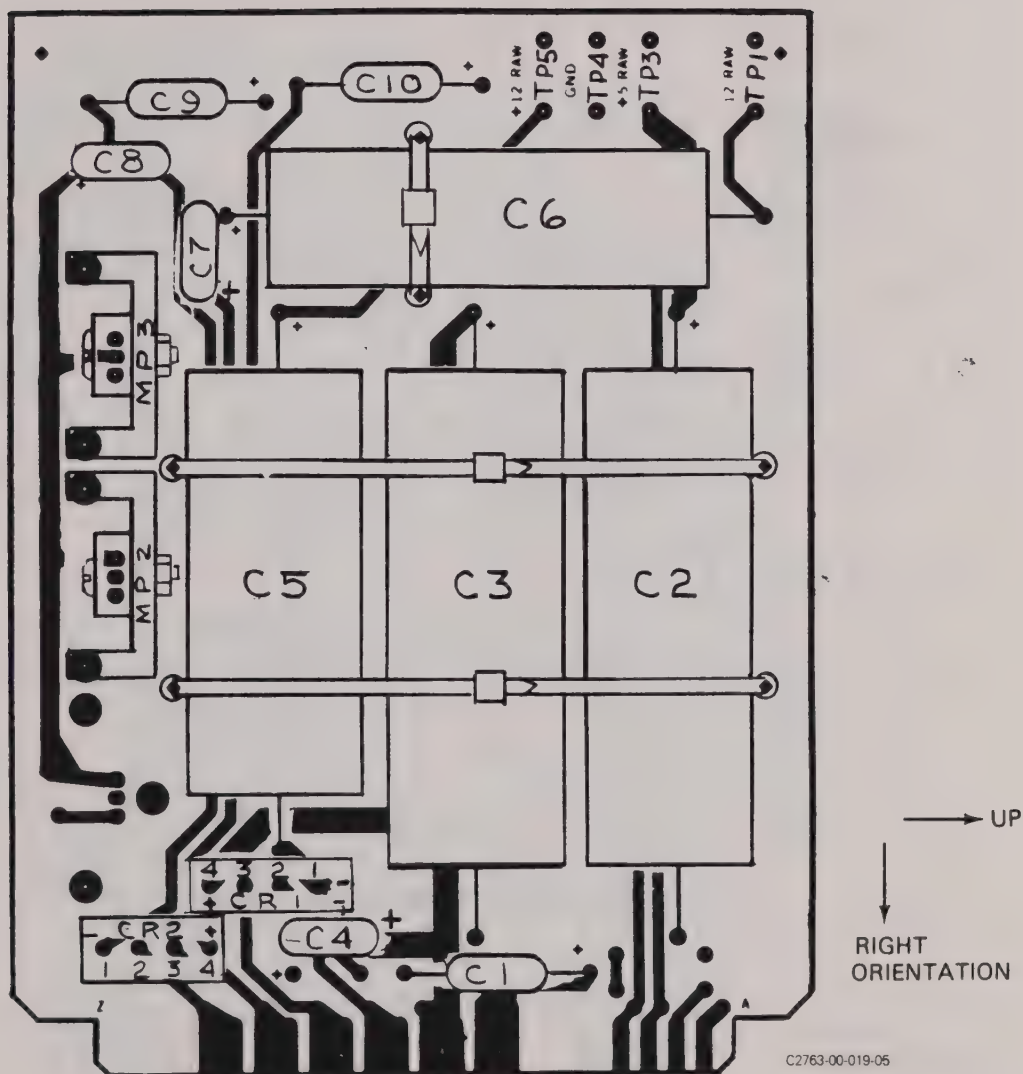


Figure 7-9. Regulator Power Supply A1 Parts Location Diagram.

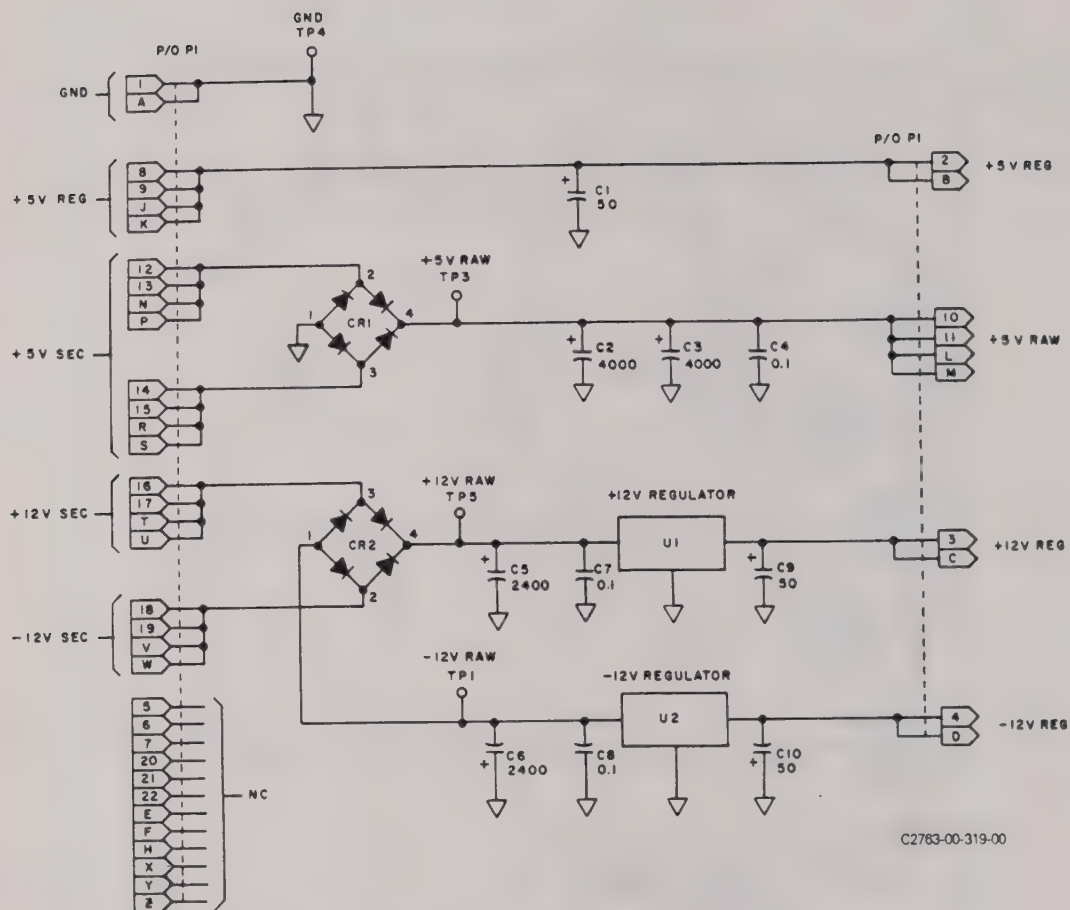
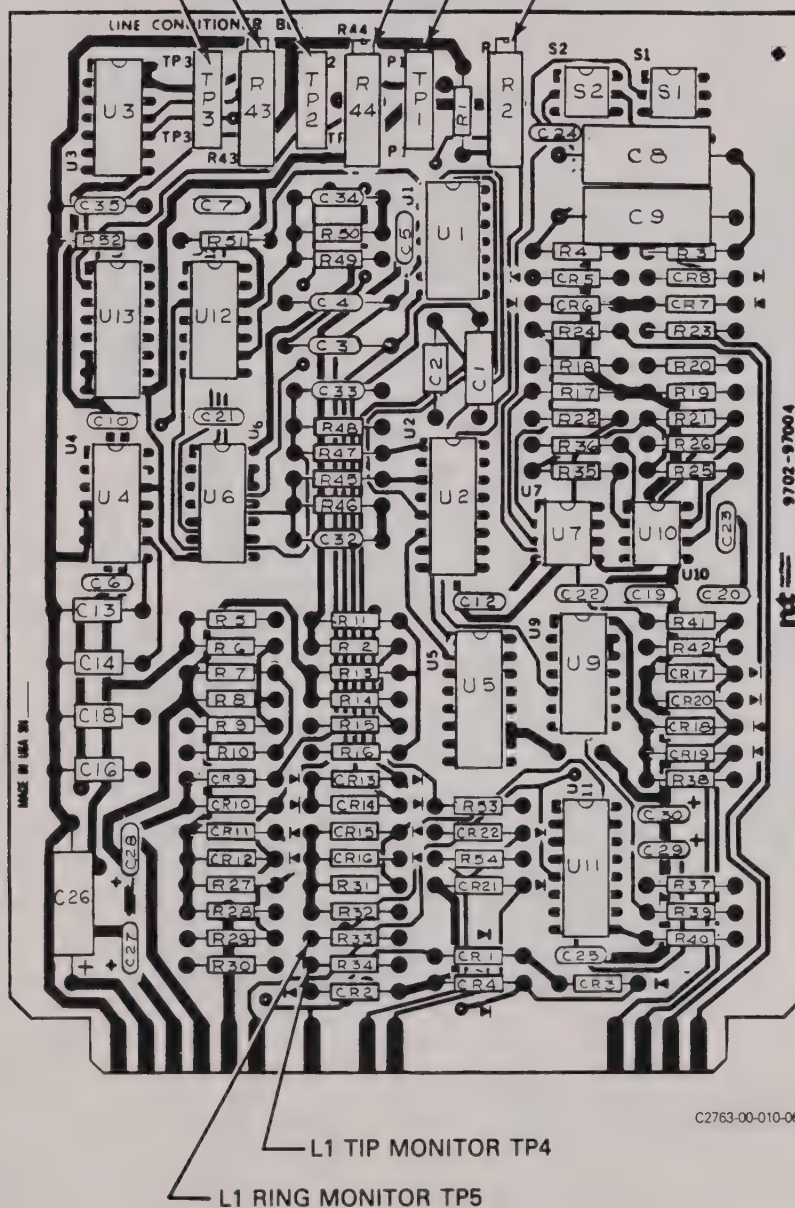


Figure 7-10. Regulator Power Supply A1 Schematic Diagram.

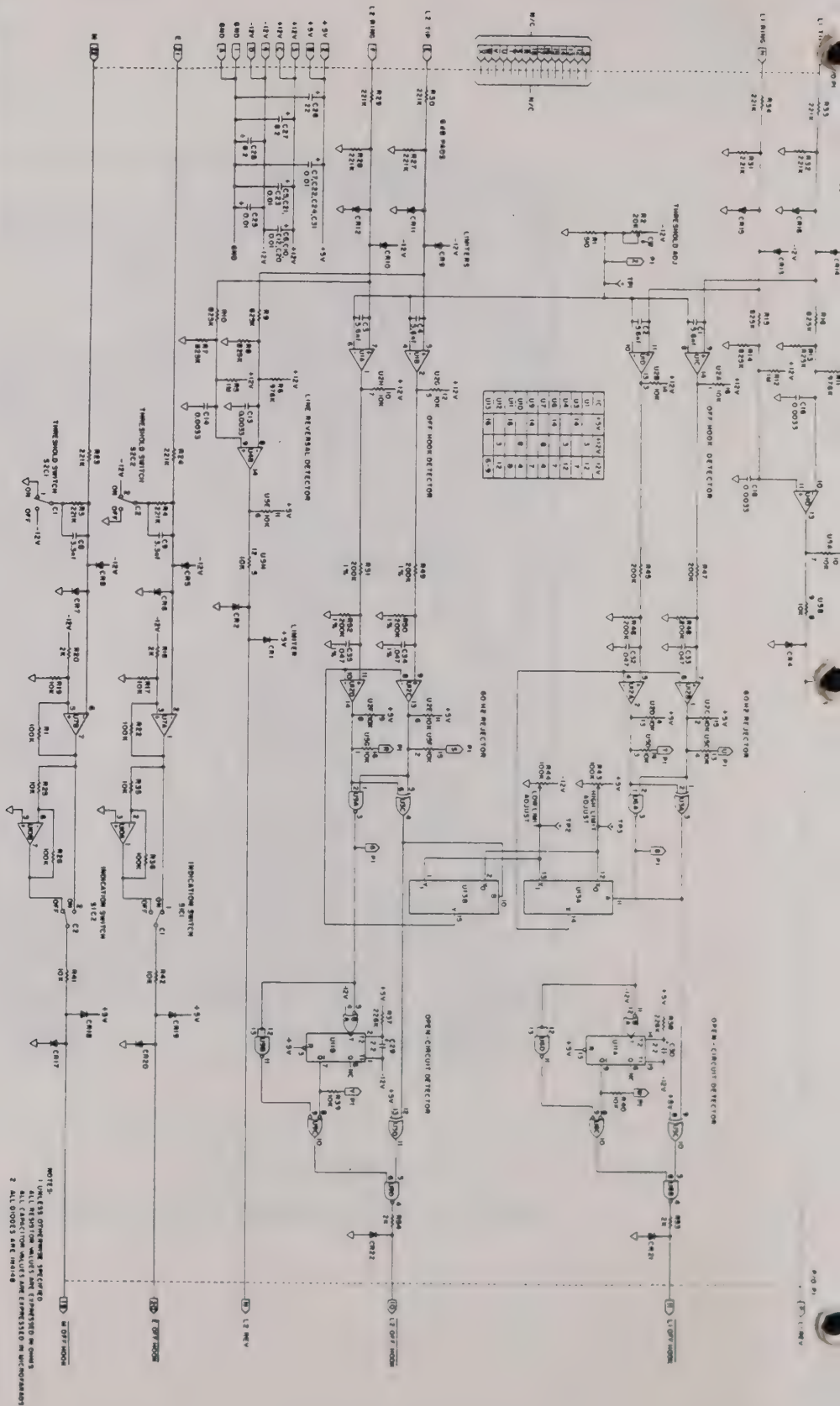
LOW LIMIT MONITOR TP2
 HIGH LIMIT ADJUST R43
 HIGH LIMIT MONITOR TP3
 LOW LIMIT ADJUST R44
 THRESHOLD MONITOR TP1
 THRESHOLD ADJUST R2



UP
 RIGHT
 ORIENTATION

Figure 7-11. Line Conditioner A3 Parts Location Diagram.

Figure 7-12. Line Conditioner A3 Schematic Diagram.



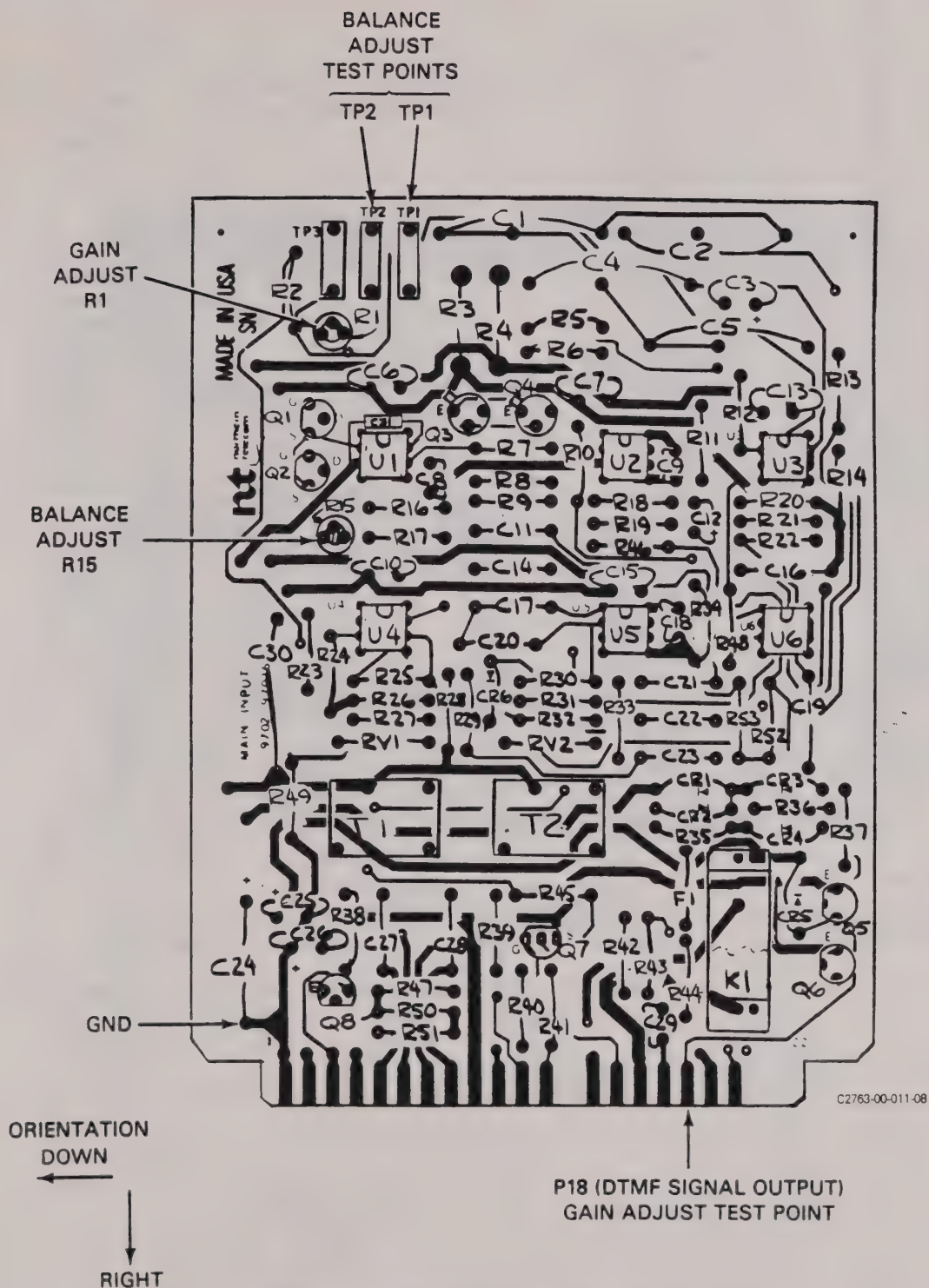


Figure 7—13. Main Input A4 Parts Location Diagram.

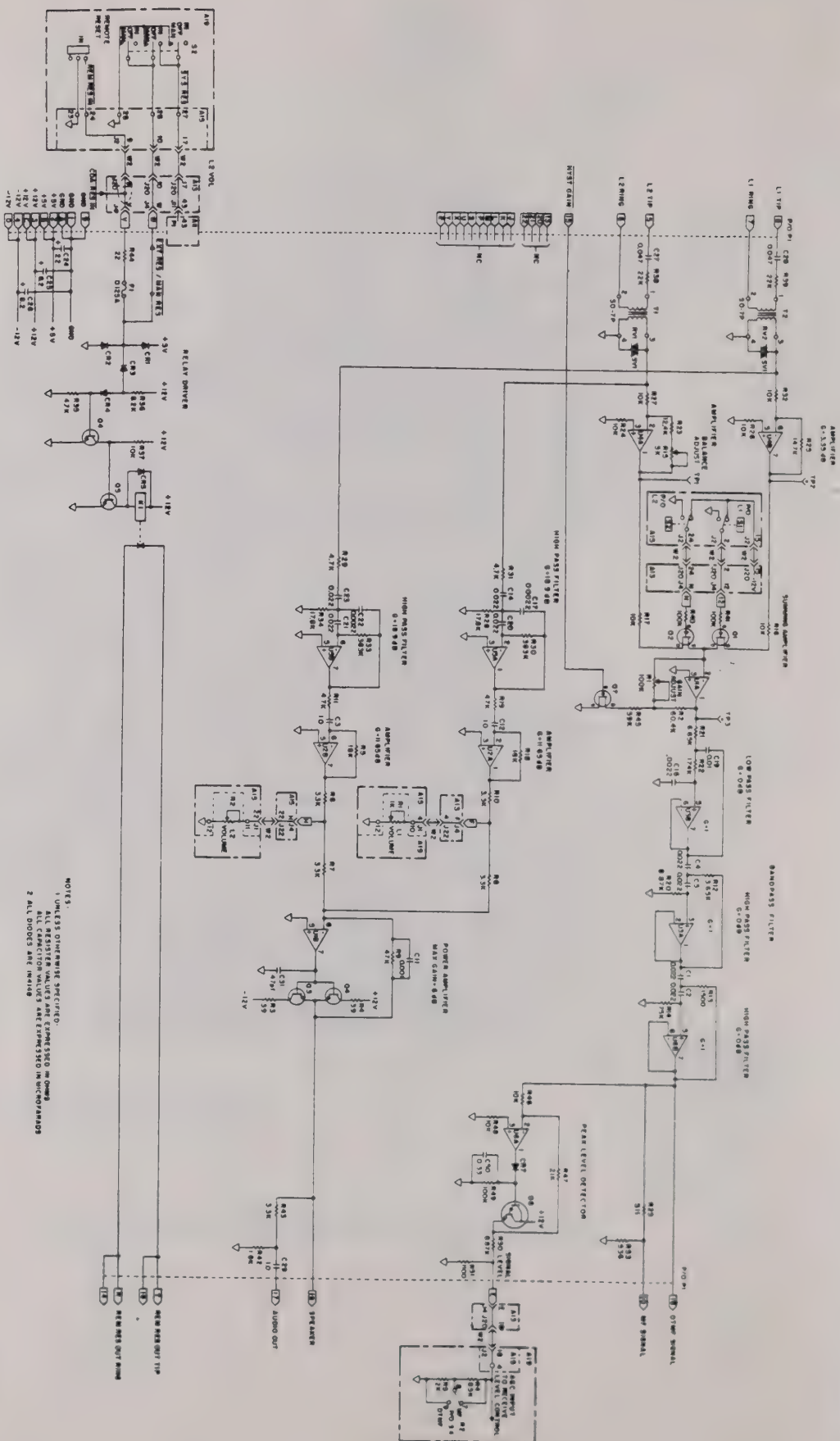


Figure 7-14. Main Input A4 Schematic Diagram.

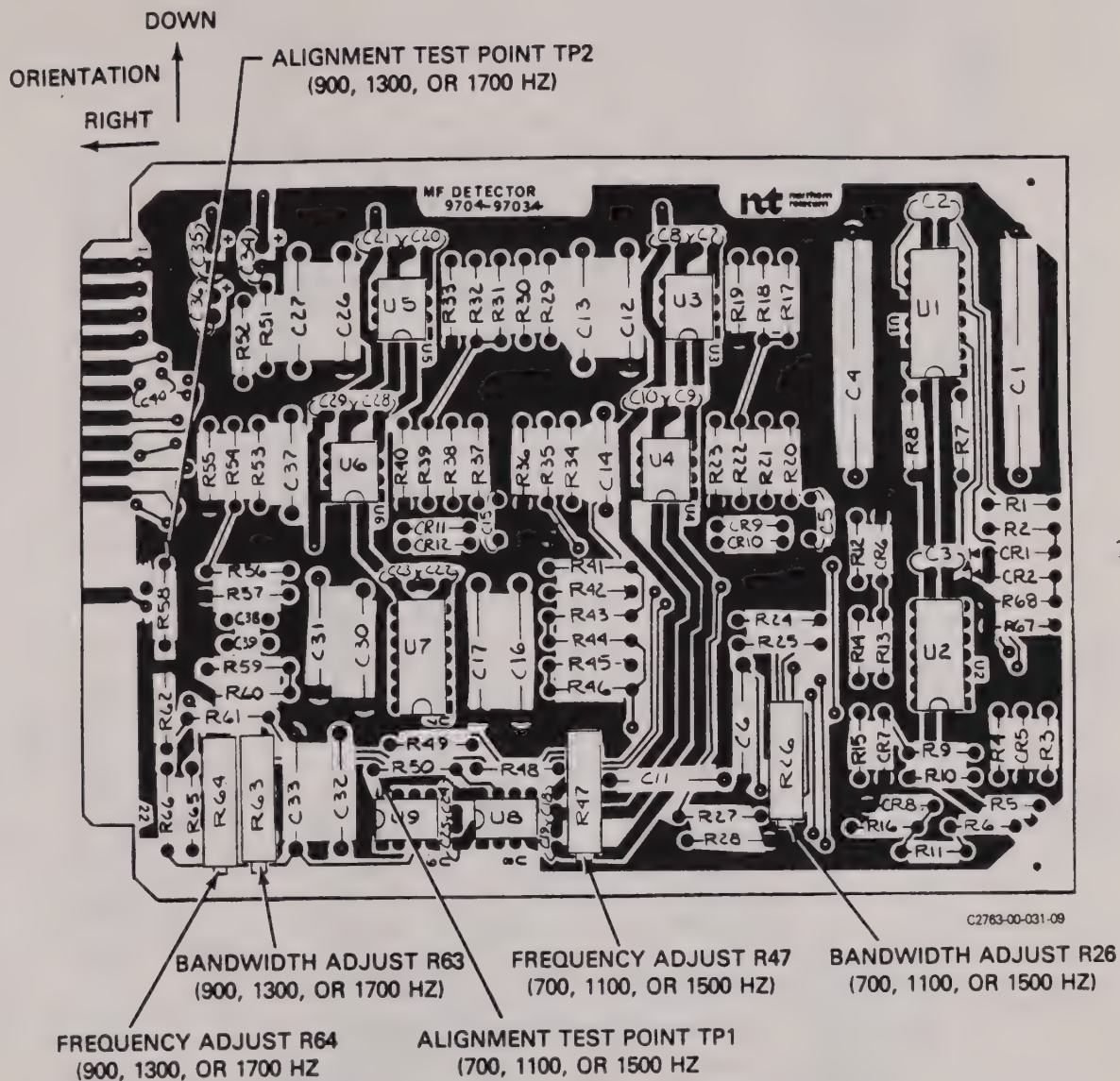


Figure 7-15. MF Detector A5, A7, and A8 Parts Location Diagram.



Schematic Diagram.

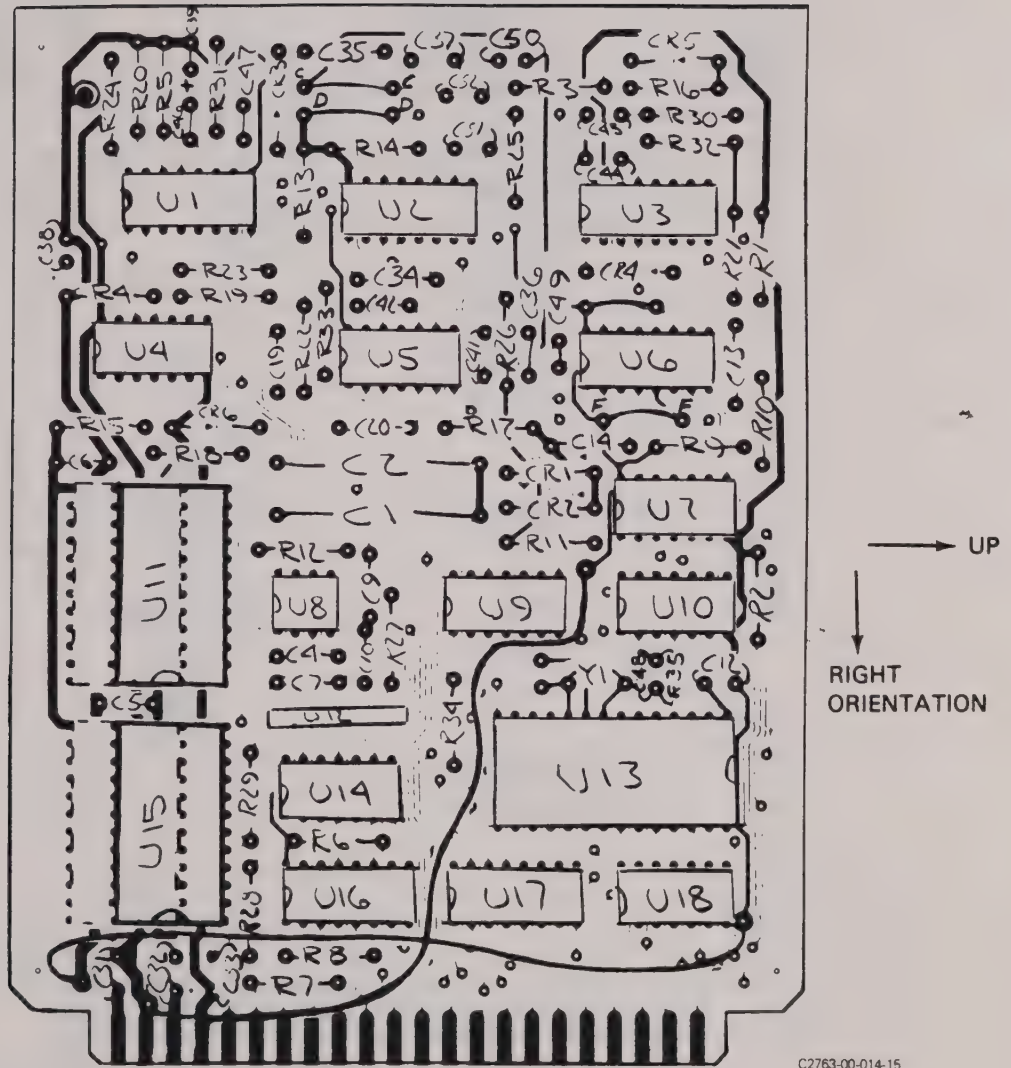


Figure 7–17. DTMF Receiver A6 Parts Location Diagram.



(MODELS 2763 AND 2763R)

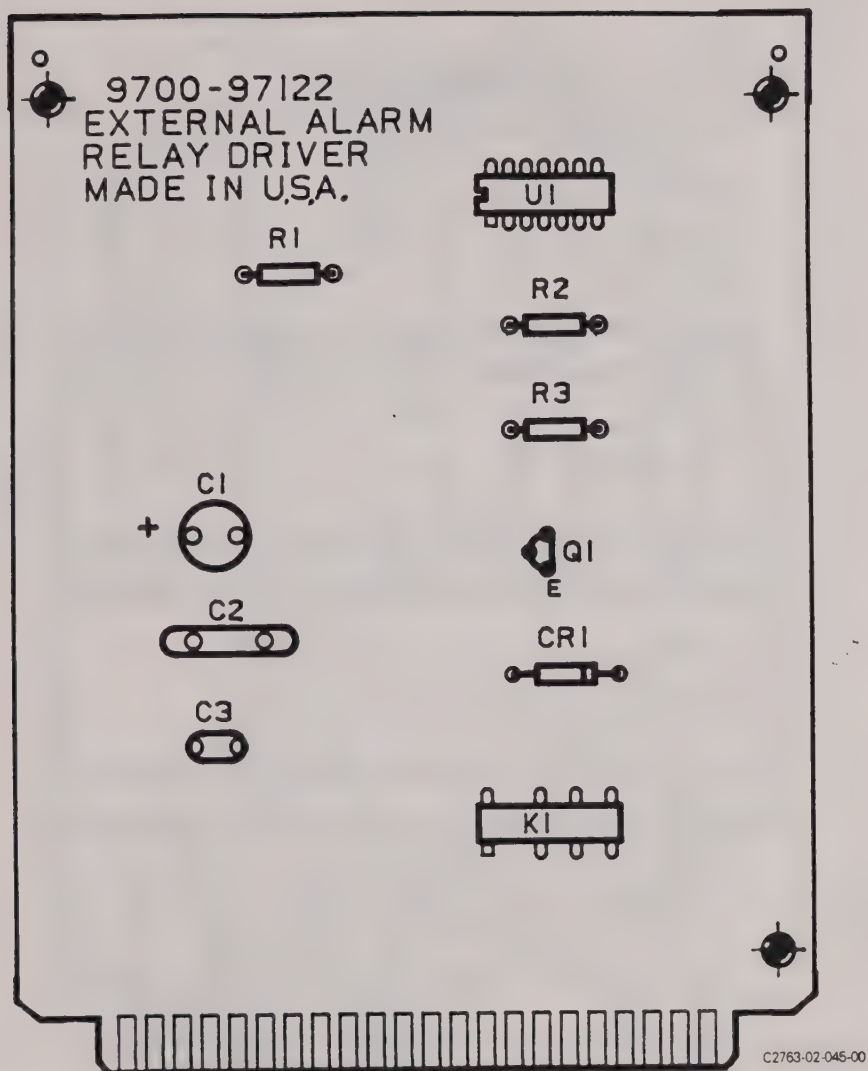


Figure 7-19. Dither Generator and Control A6 Parts Location Diagram.

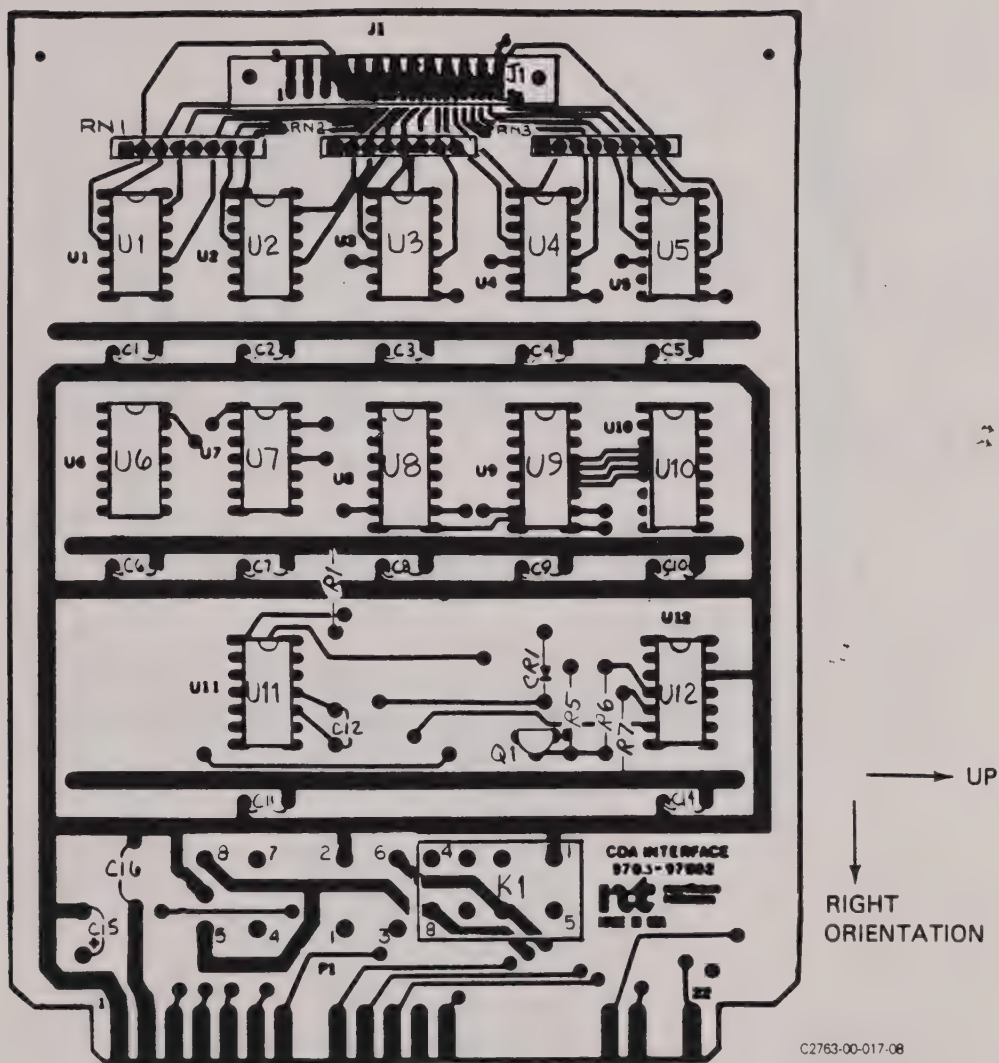


Figure 7-21. CDA Interface A10 Parts Location Diagram.

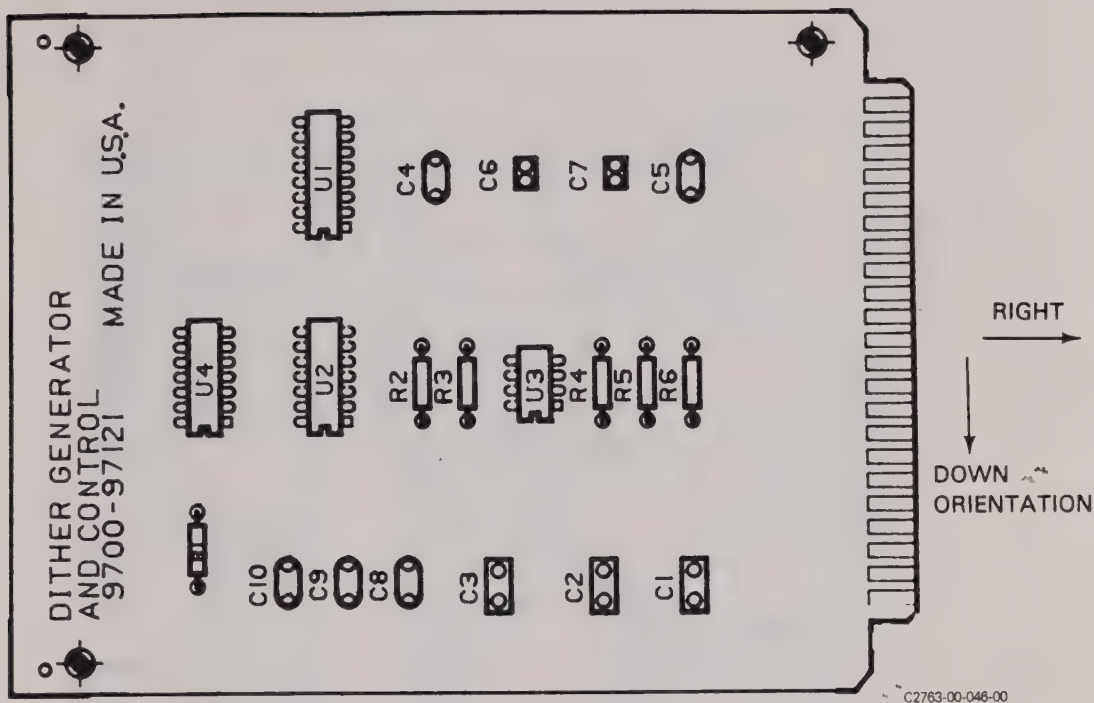
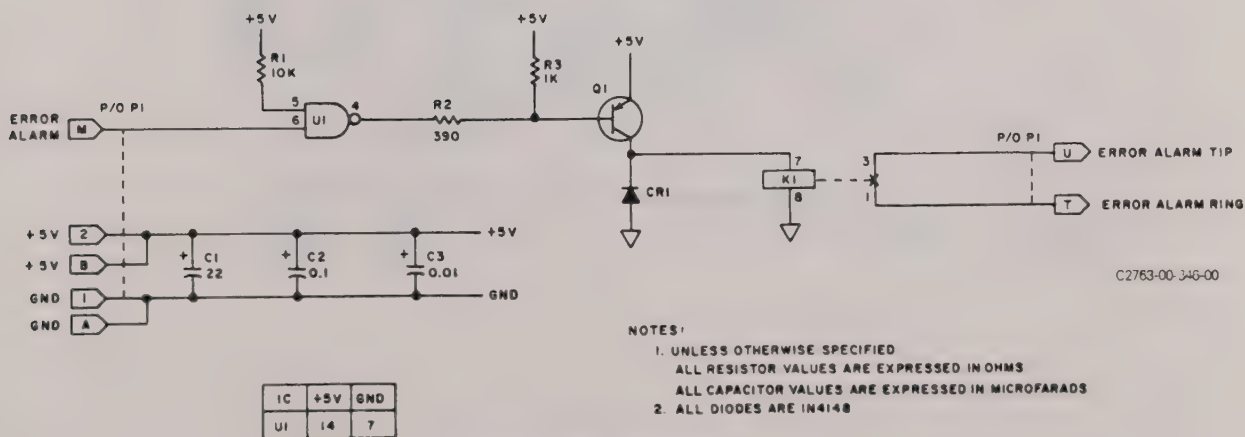


Figure 7-23. External Alarm Relay Driver A10 Parts Location Diagram.



(MODELS 2763 AND 2763A)

Figure 7-24. External Alarm Relay Driver A10 Schematic Diagram.

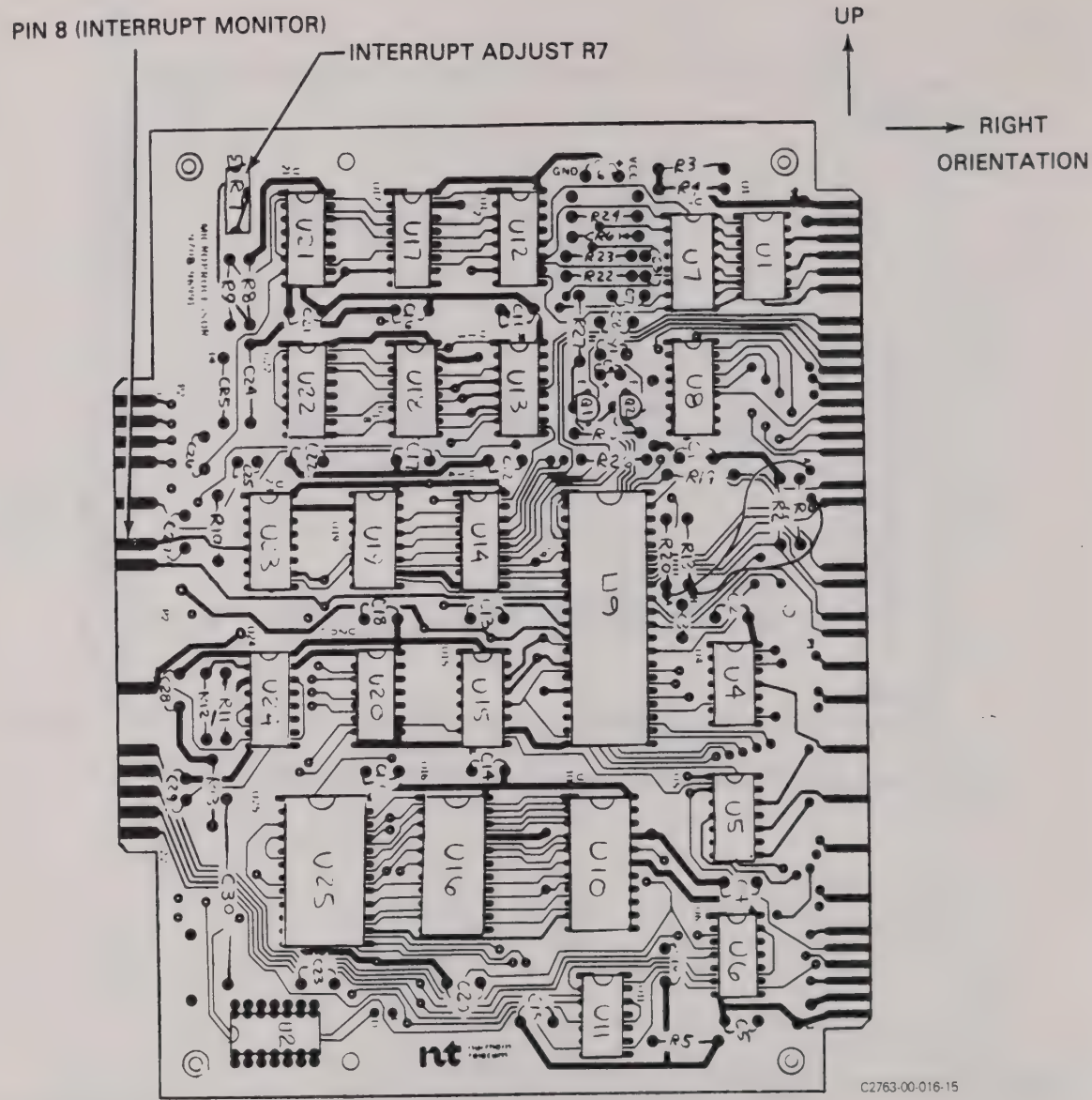


Figure 7-25. Microprocessor A11 Parts Location Diagram.

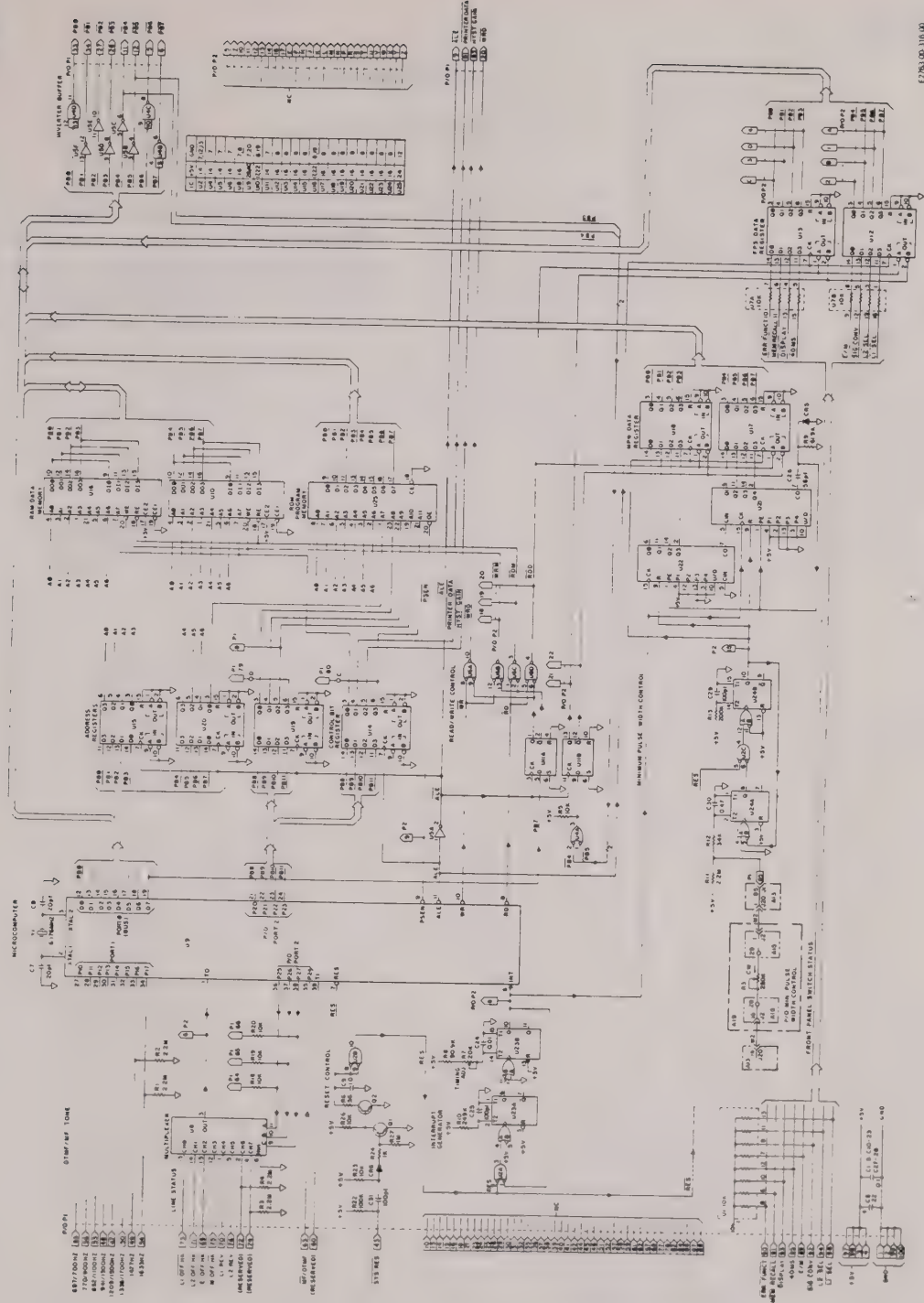


Figure 7-26. Microprocessor A11 Schematic Diagram.

SECTION 8**ELECTRONIC PARTS LISTS**

8.1 Tables 8—1 through 8—21 list the electronic parts for the Models 2763, 2763A, and 2763R Signaling Displays. The parts location diagrams contained in Section 7 show the physical locations of the reference designated items listed in this section.

Table 8--1. Overall Assembly Parts List (Model 2763).

REV 10 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
CR5-7	DIODE SIGNAL 1N4148 DIO.001 75V SI 4.0NS	560041481
R6	RESISTOR MTL-FILM 1.00 K RES.001 P 1/8W 1% 100PPMRN55	220210011
U7	RESISTOR NETWORK 8X10K DIP.16 100V 2%	514500102

Table 8--2. Overall Assembly Parts List (Model 2763A)

REV 00 DATED 7/13/82

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
A1	REGULATOR PWR SUPPLY BD	A276300019
A3	LINE COND BD	A276300010
A4	MAIN INPUT BD	A276300011
A5	MF DETECTOR 7-9	A276300031
A6	DITHER GENERATOR & CNTRL.	A276302045
A7	MF DETECTOR 11-13	A276300032
A8	MF DETECTOR 15-17	A276300033
A10	EXT.ALARM.RLY.DRVR.	A276300046
A11	MICROPRCC. BD W/FIRMWARE	A276300044
A14	CARD CAGE ASSY	A276302012
A19	SUB PNL ASSY	A276300015
W1	CABLE ASSY W1	A276300025
W2, W3	CABLE ASSY W2	A276300026

Table 8--3. Overall Assembly Parts List (Model 2763R).

REV 10 DATED 7/13/82

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
A1	REGULATOR PWR SUPPLY BD	A276300019
A3	LINE COND BD	A276300010
A4	MAIN INPUT BD	A276300011
A5	MF DETECTOR 7-9	A276300031
A6	DTMF RECEIVER BD ASSY	A276300014
A7	MF DETECTOR 11-13	A276300032
A8	MF DETECTOR 15-17	A276300033
A10	CDA I/F	A276300017
A11	MICROPROC. BD W/FIRMWARE	A276300044
A12	ACCESSORY ASSY	A276300029
A14	RACK MOUNT CARD CAGE	A276301012
A19	SUB PNL ASSY	A276300015
A20	REAR RETAINER ASSY	A276301029
A21	REAR MOUNTING PLATE ASSY	A276301027
W1	CABLE ASSY W1	A276300025
W2-3	CABLE ASSY W2	A276300026
W5	R/M CDA CABLE	A276301028

Table 8-4. Sub-Panel Assembly A19 Parts List.

REV 10 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
DS1	LED	T1.75RED	5.0V	!	16MA 60DEG 1MCD RES	564500801
J1	RECEPT, PANEL, BLK PLASTIC 3-PIN 6A 250V					652201700
J2	BINDING POST METAL GND					652500100
J3-12	JACK	PHONE	3-COND	!	OPN CKT-ENC .25" PC	650101300
R1	POTNTMTR	PLASTIC	1K-1K	VRES.523	N 1/2W 10% LIN CONCEN	238001027
R2	POTNTMTR	CARBON	10 K	VRES.520	N 1W 10% LOG-DB SW	232002542
R3	POTNTMTR	CERMET	250 K	VRES.520	N 1W 10% LINEAR SW	232002543
R4	RESISTOR	MTL-FILM	8.06 K	RES.001	P 1/8W 1% 100PPMRN55	220280611
R5	RESISTOR	MTL-FILM	2.00 K	RES.001	P 1/8W 1% 100PPMRN55	220220011
S1	SWITCH	TOGGLE	DPDT	!	ON-NONE-ON GOLD	620700001
S2	SWITCH	TOGGLE	3PDT PC	!	ON-ON-ON* GOLD	620402300
S3	DPDT LOCKING 3A 125V					645500200
S4	SWITCH	TOGGLE	3PDT	!	ON-NONE-ON GOLD	620401201

Table 8-5. Front Panel Switch Board A15 Parts List.

REV 04 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION							PART NO.
C1	CAPACITR	ELECT-AL	1.0	UF	CAP.018	N	16V -10 +75%	300201050
R1	RESISTOR	CARBON	47	R	RES.001	P	1/4W 10%	200104706
R2-7	RESISTOR	CARBON	1.0	K	RES.001	N	1/8W 10%	200001026
S1	IMP SERIES PUSH-PUSH				DPDT			635800703
S2-3	PB, IMPS	SERIES			SPST	P/P		635800702
S4	PB, IMPS	SERIES			SPST	MOM.		635800701
S5	PB, IMPS	SERIES			SPST	P/P		635800702
S6	IMP SERIES PUSH-PUSH				DPDT			635800703
S7	PB, IMPS	SERIES			SPST	MOM.		635800701
W1-2	CONNECTR	HEADER	26	DIL	!		GOLD STRAIT W/LCK	654003713

Table 8-6. Card Cage Assembly A19 Parts List.

REV 05 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
T1	TRANSFMR	POWER	P234VSP	N	S234VSP	420200300
VR1-2	INT-CKT	VOLT-REG	7805	T03	N FIXED POS 1.5A	500078051

Table 8-7. Display Assembly A18 Parts List.

REV 02 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
P1	CONNECTR D TO BD	651800701
P2	CONNECTR D TO BD	651800701

Table 8-8. Display Driver A17 Parts List.

REV 04 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
C1-3	CAPACITR CERAMIC 10 NF CAP.082 16V 20% YSP.010 UF	330701031
C4	CAPACITR ELECT-TA 100 NF CAP.036 P 35V 10% .1 UF	310001041
C5-10	CAPACITR CERAMIC 10 NF CAP.082 16V 20% YSP.010 UF	330701031
P3	CONNECTR HEADER 26 DIL ! GOLD STRAIT W/LCK	654003713
R1-2	RESISTOR CARBON 10 K RES.001 P 1/4W 10%	200101036
R3	RESISTOR CARBON 27 K RES.001 N 1/4W 5%	200102735
RN1-2	RESISTOR NETWORK 7X10K RESNET.8 100V 2%	514500010
TP1	TEST JACK R/A PC-WHITE	652900300
U1	INT-CKT TTL 74159 DIP.24 N 4-16 DECDR/DMUX/OC	510074159
U2	INT-CKT TTL 74175 DIP.16 N 4 D-TYPE F/F	510074175
U4	INT-CKT LS-TTL 74LS123 DIP.16 N RETRG MONO MULTI	510974123
U5-13	INT-CKT TTL 74175 DIP.16 N 4 D-TYPE F/F	510074175
U14	INT-CKT LS-TTL 74LS138 DIP.16 P 3-8 LINE DEC/DEMUX	510974138
U15-16	INT-CKT TTL 7404 DIP.14 N HEX INVERTER	510074040

Table 8-9. Display Board A16 Parts List.

REV 05 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
C1	CAPACITR ELECT-AL 50 UF CAP.019 N 16V -10 +75%	300205060
C2-7	CAPACITR CERAMIC 10 NF CAP.093 50V 00 Z5V.010 UF	330701030
C2-7	CAPACITR CERAMIC 10 NF CAP.082 16V 20% YSP.010 UF	330701031
CR1-20	LED T1.75RED 2.2V ! 20MA 90DEG 4MCD	564500802
Q1	TRANSSTR BJT-NPN 2N2222 T018.01 30V SI HFES0 800MA	550002222
R1-7	RESISTOR CARBON 6.8 R RES.001 N 1/4W 5%	200106895
R8	RESISTOR CARBON 270 R RES.001 P 1/4W 10%	200102716
R9	RESISTOR CARBON 6.8 R RES.001 N 1/4W 5%	200106895
R10	RESISTOR CARBON 270 R RES.001 P 1/4W 10%	200102716
RN1-4	RESISTOR NETWORK 7X270-R RESNET.8 100V 2%	514500009
TP1	TEST JACK R/A PC BLK	652900100
TP2	TEST JACK R/A PC-WHITE	652900300

Table 8-9. (Cont'd.)

REV 05 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
U1	INT-CKT	TRANSSTR	3082	DIP.16	N	HIGH CUR, COMM COL 500030820
U2	RESISTOR	NETWORK	8X47-R	DIP.16		100V 2% 514500108
U3-18	DISPLAY	LED 7SEG	0.43"	!		HI-EFF RED COM CATH 728301703
U19	INT-CKT	DRIVER	2003	DIP.16	N	7CHN CMOS/TTL INPUT 510075468
U20	INT-CKT	TTL	7404	DIP.14	N	HEX INVERTER 510074040
U21	INT-CKT	DRIVER	2003	DIP.16	N	7CHN CMOS/TTL INPUT 510075468
U22	INT-CKT	TTL	7404	DIP.14	N	HEX INVERTER 510074040
U23	INT-CKT	DRIVER	2003	DIP.16	N	7CHN CMOS/TTL INPUT 510075468
U24	INT-CKT	TTL	7404	DIP.14	N	HEX INVERTER 510074040
XU3-18	SOCKET	PC MOUNT	14 DIL	!		.300 .150HT TIN 820100300

Table 8-10. Interconnect A13 Parts List.

REV 08 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
J1-10	CONNECTR	CARDEDGE	22PDUAL	!		GOLD PC DIP SOLDER 651701200
J11	CONNECTOR,	CARD EDGE		50 POS		651800010
J20-21	CONNECTR	HEADER	26 DIL	!		GOLD STRAIT W/LCK 654003713
J22	CONNECTR	HEADER	26 DIL	!		STRAIT GOLD SOLDER 654002101
TP1	TEST JACK	R/A	PC BLK			652900100
TP2-4	TEST JACK	R/A	PC-WHITE			652900300

Table 8-11. Regulator Power Supply A1 Parts List.

REV 06 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
C1	CAPACITR	ELECT-AL	50 UF	CAP.023	P	25V -10 +75% 300205062
C2-3	CAPACITR	ELECT-AL	4000 UF	CAP.015	P	25V -10 +50% 300004080
C4	CAPACITR	CERAMIC	100 NF	CAP.085		75V 00 25V.1 UF 330201040
C5-6	CAPACITR	ELECT-AL	2400 UF	CAP.003	P	30V -10 +75% 300002480
C7-8	CAPACITR	CERAMIC	100 NF	CAP.085		75V 00 25V.1 UF 330201040
C9-10	CAPACITR	ELECT-AL	50 UF	CAP.023	P	25V -10 +75% 300205062
CR1-2	DIODE	BRIDGE	MDA970			565000001
MP2-3	HEATSINK,	PC MTG,	TO-220			650000001
TP1	TEST JACK	R/A	PC-WHITE			652900300
TP3	TEST JACK	R/A	PC-WHITE			652900300
TP4	TEST JACK	R/A	PC BLK			652900100
TP5	TEST JACK	R/A	PC-WHITE			652900300
U1	INT-CKT	VOLT-REG	7812	T0220	P	FIXED POS 1 AMP 500000340
U2	INT-CKT	VOLT-REG	7912	T0220	P	FIXED NEG 1AMP 500000320

Table 8-12. Line Conditioner A3 Parts List.

REV 07 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
C1-4	CAPACITR	POLYESTR	5.6	NF	CAP.043	P	100V	10%	5600	PF	320005620
C5-7	CAPACITR	CERAMIC	10	NF	CAP.093		50V	00	Z5V.010	UF	330701030
C8-9	CAPACITR	POLYESTR	3.3	NF	CAP.043	P	100V	10%	3300	PF	320003320
C10	CAPACITR	CERAMIC	10	NF	CAP.093		50V	00	Z5V.010	UF	330701030
C12	CAPACITR	CERAMIC	10	NF	CAP.093		50V	00	Z5V.010	UF	330701030
C13-14	CAPACITR	POLYESTR	3.3	NF	CAP.043	P	100V	10%	3300	PF	320003320
C16	CAPACITR	POLYESTR	3.3	NF	CAP.043	P	100V	10%	3300	PF	320003320
C18	CAPACITR	POLYESTR	3.3	NF	CAP.043	P	100V	10%	3300	PF	320003320
C19-25	CAPACITR	CERAMIC	10	NF	CAP.093		50V	00	Z5V.010	UF	330701030
C26	CAPACITR	ELECT-TA	22	UF	CAP.032	N	15V	10%			310302260
C27-28	CAPACITR	ELECT-TA	8.2	UF	CAP.036	N	15V	10%			310008250
C29-30	CAPACITR	ELECT-TA	2.2	UF	CAP.036	P	35V	10%			310002250
C31	CAPACITR	CERAMIC	10	NF	CAP.093		50V	00	Z5V.010	UF	330701030
C32-35	CAPACITR	T-P-PROP	47	NF	CAP.075	N	100V	1%	.047	UF	322304731
CR1-22	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS		560041480
R1	RESISTOR	CARBON	510	R	RES.003	N	1/2W	5%			200205115
R2	TRIM-POT	CERM-1ST	20	K	VRES.001	P	3/4W	10%	END-ADJ		232502030
R3-4	RESISTOR	MTL-FILM	221	K	RES.001	P	1/8W	1%	100PPMRN55		220222131
R5	RESISTOR	MTL-FILM	1.00	M	RES.001	P	1/8W	1%	100PPMRN55		220210041
R6	RESISTOR	MTL-FILM	976	K	RES.001	P	1/8W	1%	100PPMRN55		220297631
R7-10	RESISTOR	MTL-FILM	806	K	RES.001	P	1/8W	1%	100PPMRN55		220280631
R7-10	RESISTOR	MTL-FILM	825	K	RES.001	P	1/8W	1%	100PPMRN55		220282531
R11	RESISTOR	MTL-FILM	976	K	RES.001	P	1/8W	1%	100PPMRN55		220297631
R12	RESISTOR	MTL-FILM	1.00	M	RES.001	P	1/8W	1%	100PPMRN55		220210041
R13-16	RESISTOR	MTL-FILM	806	K	RES.001	P	1/8W	1%	100PPMRN55		220280631
R13-16	RESISTOR	MTL-FILM	825	K	RES.001	P	1/8W	1%	100PPMRN55		220282531
R17	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55		220210021
R18	RESISTOR	MTL-FILM	2.00	K	RES.001	P	1/8W	1%	100PPMRN55		220220011
R19	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55		220210021
R20	RESISTOR	MTL-FILM	2.00	K	RES.001	P	1/8W	1%	100PPMRN55		220220011
R21-22	RESISTOR	MTL-FILM	100	K	RES.001	P	1/8W	1%	100PPMRN55		220210031
R23-24	RESISTOR	MTL-FILM	221	K	RES.001	P	1/8W	1%	100PPMRN55		220222131
R25	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55		220210021
R26	RESISTOR	MTL-FILM	100	K	RES.001	P	1/8W	1%	100PPMRN55		220210031
R27-34	RESISTOR	MTL-FILM	221	K	RES.001	P	1/8W	1%	100PPMRN55		220222131
R35	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55		220210021
R36	RESISTOR	MTL-FILM	100	K	RES.001	P	1/8W	1%	100PPMRN55		220210031
R37-38	RESISTOR	MTL-FILM	226	K	RES.001	P	1/8W	1%	100PPMRN55		220222631
R39-42	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R43-44	TRIM-POT	CERM-1ST	100	K	VRES.001	P	3/4W	10%	END-ADJ		232501040
R45-52	RESISTOR	MTL-FILM	200	K	RES.001	P	1/8W	1%	100PPMRN55		220220031
R53-54	RESISTOR	CARBON	2.0	K	RES.001	N	1/4W	5%			200102025
S1-2	DIP SWITCH,2 FORM C										640001300
TP1	TEST JACK R/A PC-WHITE										652900300
TP2	TEST JACK R/A PC BLK										652900100
TP3	TEST JACK R/A PC-WHITE										652900300
U1	INT-CKT	COMPARTR	339		DIP.14	P	QUAD	5-36V			500000339
U2	RESISTOR	NETWORK	8X10K		DIP.16		100V	2%			514500102
U3	INT-CKT	CMOS	4070BUF		DIP.14	P	4X2	IN EXC-OR GTE			510004070
U4	INT-CKT	COMPARTR	339		DIP.14	P	QUAD	5-36V			500000339
U5	RESISTOR	NETWORK	8X10K		DIP.16		100V	2%			514500102
U6	INT-CKT	CMOS	4011BUF		DIP.14	P	4X2	IN NAND GATE			510004011
U7	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL	741C			500001458
U9	INT-CKT	CMOS	4011BUF		DIP.14	P	4X2	IN NAND GATE			510004011
U10	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL	741C			500001458
U11	INT-CKT	CMOS	4538BUF		DIP.16	P	2X	PRC MONO MLTIVI			510004538

Table 8-12. (Cont'd.)

REV 07 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
U12	INT-CKT	COMPARTR	339	DIP.14	P	QUAD 5-36V 500000339
U13	INT-CKT	CMOS	4053BUF	DIP.16	P	3X2CHN ALG MUX/DEMU 510004053

Table 8-13. Main Input A4 Parts List.

REV 10 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
C1-2	CAPACITR	A-P-PROP	22	NF	P	100V 1% .022 UF 322402230
C3	CAPACITR	ELECT-TA	1.0	UF	CAP.036	P 35V 10% 310001051
C4-5	CAPACITR	A-P-PROP	22	NF	P	100V 1% .022 UF 322402230
C6-10	CAPACITR	CERAMIC	10	NF	CAP.093	50V 00 Z5V.010 UF 330701030
C11	CAPACITR	POLYESTR	1.0	NF	CAP.043	P 100V 10% 1000 PF 320001020
C12	CAPACITR	ELECT-TA	1.0	UF	CAP.036	P 35V 10% 310001051
C13	CAPACITR	CERAMIC	10	NF	CAP.093	50V 00 Z5V.010 UF 330701030
C14	CAPACITR	POLYESTR	22	NF	CAP.043	P 100V 10% .022 UF 320002230
C15	CAPACITR	CERAMIC	10	NF	CAP.093	50V 00 Z5V.010 UF 330701030
C16	CAPACITR	POLYSTYR	2.2	NF	CAP.059	N 100V 1% 2200 PF 321502220
C17	CAPACITR	POLYESTR	2.2	NF	CAP.043	P 100V 10% 2200 PF 320002220
C18	CAPACITR	CERAMIC	10	NF	CAP.093	50V 00 Z5V.010 UF 330701030
C19	CAPACITR	POLYSTYR	10	NF	CAP.018	N 100V 2% .010 UF 321501032
C20-21	CAPACITR	POLYESTR	22	NF	CAP.043	P 100V 10% .022 UF 320002230
C22	CAPACITR	POLYESTR	2.2	NF	CAP.043	P 100V 10% 2200 PF 320002220
C23	CAPACITR	POLYESTR	22	NF	CAP.043	P 100V 10% .022 UF 320002230
C24	CAPACITR	ELECT-TA	22	UF	CAP.032	N 15V 10% 310302260
C25-26	CAPACITR	ELECT-TA	8.2	UF	CAP.036	N 15V 10% 310008250
C27-28	CAPACITR	POLYESTR	47	NF	CAP.043	P 100V 10% .047 UF 320004730
C29	CAPACITR	CERAMIC	1.0	UF	CAP.037	50V 20% Y5V 330801050
C30	CAPACITR	M-P-ESTR	330	NF	CAP.018	N 100V 1% .33 UF 321903341
C31	CAPACITR	SIL-MICA	47	PF	CAP.091	N 100V 5% 335404700
CR1-6	DIODE	SIGNAL	1N4148	DIO.001		75V SI 4.0NS 560041480
F1	FUSE	SUB-MINI	1/8A	!		125V AXIAL LEAD 863200900
K1	RELAY	DRY-REED	12V 1A	!		.5A 2K PC 9.6V/1.2V 604101300
Q1-2	TRANSSTR	JFET-NCH	T1S73	T092-M		30V SI 554000730
Q3	TRANSSTR	BJT-PNP	2N4036	T05.01		65V SI HFE20 1A 552040360
Q4	TRANSSTR	BJT-NPN	2N2102	T05.01		65V SI HFE40 1A 550021020
Q5-6	TRANSSTR	BJT-NPN	2N3903	T092.01		40V SI HFE50 200MA 550039030
Q7	TRANSSTR	JFET-PCH	2N5463	T092		60V SI 555005463
Q8	TRANSSTR	DAR-NPN	MPSA12	T092.03		20V SI HFE20K 0.5A 550000120
R1	TRIM-POT	CERM-1T	100	K	VRES.011	N 1/2W 10% TOP-ADJ 232701046
R2	RESISTOR	MTL-FILM	60.4	K	RES.001	P 1/8W 1% 100PPMRN55 220260421
R3-4	RESISTOR	CARBON	39	R	RES.003	N 1/2W 5% 200203905
R5	RESISTOR	CARBON	18	K	RES.001	P 1/4W 10% 200101836
R6-8	RESISTOR	CARBON	3.3	K	RES.001	P 1/4W 10% 200103326
R9	RESISTOR	CARBON	47	K	RES.001	P 1/4W 10% 200104736
R10	RESISTOR	CARBON	3.3	K	RES.001	P 1/4W 10% 200103326
R11	RESISTOR	CARBON	4.7	K	RES.001	P 1/4W 10% 200104726
R12	RESISTOR	MTL-FILM	3.65	K	RES.001	P 1/8W 1% 100PPMRN55 220236511
R13	RESISTOR	MTL-FILM	1.50	K	RES.001	P 1/8W 1% 100PPMRN55 220215011
R14	RESISTOR	MTL-FILM	75.0	K	RES.001	P 1/8W 1% 100PPMRN55 220275021
R15	TRIM-POT	CERM-1T	5.0	K	VRES.011	N 1/2W 10% TOP-ADJ 232705026
R16-17	RESISTOR	MTL-FILM	10.0	K	RES.001	P 1/8W 1% 100PPMRN55 220210021
R18	RESISTOR	CARBON	18	K	RES.001	P 1/4W 10% 200101836
R19	RESISTOR	CARBON	4.7	K	RES.001	P 1/4W 10% 200104726

Table 8-13. (Cont'd.)

REV 10 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
R20	RESISTOR	MTL-FILM	8.87	K	RES.001	P	1/8W	1%	100PPMRN55	220288711	
R21	RESISTOR	MTL-FILM	6.65	K	RES.001	P	1/8W	1%	100PPMRN55	220266511	
R22	RESISTOR	MTL-FILM	17.4	K	RES.001	P	1/8W	1%	100PPMRN55	220217421	
R23	RESISTOR	MTL-FILM	12.4	K	RES.001	P	1/8W	1%	100PPMRN55	220212421	
R24	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55	220210021	
R25	RESISTOR	MTL-FILM	14.7	K	RES.001	P	1/8W	1%	100PPMRN55	220214721	
R26-27	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55	220210021	
R28	RESISTOR	MTL-FILM	17.8	K	RES.001	P	1/8W	1%	100PPMRN55	220217821	
R29	RESISTOR	CARBON	4.7	K	RES.001	P	1/4W	10%		200104726	
R30	RESISTOR	MTL-FILM	383	K	RES.001	P	1/8W	1%	100PPMRN55	220238331	
R31	RESISTOR	CARBON	4.7	K	RES.001	P	1/4W	10%		200104726	
R32	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55	220210021	
R33	RESISTOR	MTL-FILM	383	K	RES.001	P	1/8W	1%	100PPMRN55	220238331	
R34	RESISTOR	MTL-FILM	17.8	K	RES.001	P	1/8W	1%	100PPMRN55	220217821	
R35	RESISTOR	CARBON	4.7	K	RES.001	P	1/4W	10%		200104726	
R36	RESISTOR	CARBON	8.2	K	RES.001	P	1/4W	10%		200108226	
R37	RESISTOR	CARBON	10	K	RES.001	P	1/4W	10%		200101036	
R38-39	RESISTOR	CARBON	22	K	RES.001	P	1/4W	10%		200102236	
R40-41	RESISTOR	CARBON	100	K	RES.001	P	1/4W	10%		200101046	
R42	RESISTOR	CARBON	1.8	K	RES.001	P	1/4W	10%		200101826	
R43	RESISTOR	CARBON	3.3	K	RES.001	P	1/4W	10%		200103326	
R44	RESISTOR	CARBON	22	R	RES.001	P	1/4W	10%		200102206	
R45	RESISTOR	MTL-FILM	59.0	K	RES.001	P	1/8W	1%	100PPMRN55	220259021	
R46	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55	220210021	
R47	RESISTOR	MTL-FILM	21.0	K	RES.001	P	1/8W	1%	100PPMRN55	220221021	
R48	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55	220210021	
R49	RESISTOR	CARBON	100	K	RES.001	P	1/4W	10%		200101046	
R50	RESISTOR	MTL-FILM	8.87	K	RES.001	P	1/8W	1%	100PPMRN55	220288711	
R51	RESISTOR	MTL-FILM	1.10	K	RES.001	P	1/8W	1%	100PPMRN55	220211011	
R52	RESISTOR	MTL-FILM	511	R	RES.001	P	1/8W	1%	100PPMRN55	220251101	
R53	RESISTOR	MTL-FILM	536	R	RES.001	P	1/8W	1%	100PPMRN55	220253601	
RV1-2	VARISTOR	SILICON	SU-1								565510000
T1-2	TRANSFMR	COUPLING	P12KSP		XFMR.017	N	S30KSP	200-20KHZ			400300100
TP1-3	TEST JACK	R/A	PC-WHITE								652900300
U1-6	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL	741C			500001458

Table 8-14. MF Detector A5 Parts List.

REV 09 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
C1	CAPACITR	POLYSTYR	22	NF	CAP.018	N	100V	2%	.022	UF	321502230
C2-3	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C4	CAPACITR	POLYSTYR	22	NF	CAP.018	N	100V	2%	.022	UF	321502230
C5	CAPACITR	CERAMIC	10	PF	CAP.082		1KV	10%	N330		330001000
C6	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027	UF	322902741
C7-10	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C11-13	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027	UF	322902741
C14	CAPACITR	POLYESTR	150	NF		N	250V	10%	.15	UF	320215421
C15	CAPACITR	CERAMIC	10	PF	CAP.082		1KV	10%	N330		330001000
C16-17	CAPACITR	ELECT-NP	4.7	UF	CAP.032	N	25V	-10	+100% N-P		301304750
C18-25	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C26-27	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027	UF	322902741
C28-29	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C30-31	CAPACITR	ELECT-TA	10	UF	CAP.032	N	20V	10%			310301060

Table 8-14 (Cont'd.)

REV 09 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
C32-33	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027	UF	322902741
C34-36	CAPACITR	ELECT-TA	10	UF	CAP.042	N	20V	20%			310801060
C37	CAPACITR	POLYESTR	150	NF		N	250V	10%	.15	UF	320215421
C38-39	CAPACITR	CERAMIC	680	PF	CAP.082		1KV	10%	Z5R		330006810
C40	CAPACITR	CERAMIC	220	NF	CAP.037		50V	20%	Y5V.22	UF	330802240
CR1-2	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS		560041480
CR5-12	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS		560041480
R1-3	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			200001046
R4-6	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R7-8	RESISTOR	MTL-FILM	82.5	K	RES.001	P	1/8W	1%	100PPMRN55		220282521
R9	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			200001046
R10	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R11	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			200001046
R12	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R13	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			200001046
R14-16	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R17-19	RESISTOR	MTL-FILM	6.49	K	RES.001	N	1/8W	.25	50PPM-RN55		222164910
R20-22	RESISTOR	MTL-FILM	28.0	K	RES.001	P	1/8W	1%	100PPMRN55		220228021
R23	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R24	RESISTOR	MTL-FILM	8.45	K	RES.001	P	1/8W	1%	100PPMRN55		220284511
R25	RESISTOR	MTL-FILM	64.9	K	RES.001	P	1/8W	1%	100PPMRN55		220264921
R26	TRIM-POT	CERM-1ST	20	K	VRES.001	P	3/4W	10%	END-ADJ		232502030
R27-28	RESISTOR	MTL-FILM	8.45	K	RES.001	P	1/8W	1%	100PPMRN55		220284511
R29	RESISTOR	MTL-FILM	6.49	K	RES.001	N	1/8W	.25	50PPM-RN55		222164910
R30	RESISTOR	MTL-FILM	59.0	K	RES.001	P	1/8W	1%	100PPMRN55		220259021
R31-33	RESISTOR	MTL-FILM	8.45	K	RES.001	N	1/8W	.25	100PPMRN55		220484518
R34	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R35	RESISTOR	MTL-FILM	34.0	K	RES.001	P	1/8W	1%	100PPMRN55		220234021
R36	RESISTOR	MTL-FILM	7.15	K	RES.001	P	1/8W	1%	100PPMRN55		220271511
R37-39	RESISTOR	MTL-FILM	28.0	K	RES.001	P	1/8W	1%	100PPMRN55		220228021
R40	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R41-46	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55		220210021
R47	TRIM-POT	CERM-1ST	1.0	K	VRES.001	P	3/4W	10%	END-ADJ		232501020
R48	RESISTOR	MTL-FILM	7.87	K	RES.001	P	1/8W	1%	100PPMRN55		220278711
R49	RESISTOR	MTL-FILM	6.04	K	RES.001	P	1/8W	1%	100PPMRN55		220260411
R50	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R51	RESISTOR	MTL-FILM	8.45	K	RES.001	N	1/8W	.25	100PPMRN55		220484518
R52	RESISTOR	MTL-FILM	59.0	K	RES.001	P	1/8W	1%	100PPMRN55		220259021
R53	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R54	RESISTOR	MTL-FILM	34.0	K	RES.001	P	1/8W	1%	100PPMRN55		220234021
R55	RESISTOR	MTL-FILM	7.15	K	RES.001	P	1/8W	1%	100PPMRN55		220271511
R56	RESISTOR	MTL-FILM	499	R	RES.001	P	1/8W	1%	100PPMRN55		220249901
R57	RESISTOR	MTL-FILM	2.05	K	RES.001	P	1/8W	1%	100PPMRN55		220220511
R58	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R59	RESISTOR	MTL-FILM	499	R	RES.001	P	1/8W	1%	100PPMRN55		220249901
R60	RESISTOR	MTL-FILM	2.05	K	RES.001	P	1/8W	1%	100PPMRN55		220220511
R61-62	RESISTOR	MTL-FILM	6.49	K	RES.001	P	1/8W	1%	100PPMRN55		220264911
R63	TRIM-POT	CERM-1ST	20	K	VRES.001	P	3/4W	10%	END-ADJ		232502030
R64	TRIM-POT	CERM-1ST	1.0	K	VRES.001	P	3/4W	10%	END-ADJ		232501020
R65	RESISTOR	MTL-FILM	64.9	K	RES.001	P	1/8W	1%	100PPMRN55		220264921
R66	RESISTOR	MTL-FILM	6.49	K	RES.001	P	1/8W	1%	100PPMRN55		220264911
R67-68	RESISTOR	MTL-FILM	499	K	RES.001	P	1/8W	1%	100PPMRN55		220249931
U1	INT-CKT	CMOS	4538BUF		DIP.16	P	2X PRC MONO MLTIVI				510004538
U2	INT-CKT	CMOS	4093BUF		DIP.14	P	4X2 IN NAND SCHM TR				510004093
U3-6	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL 741C				500001458
U7	INT-CKT	COMPARTR	339		DIP.14	P	QUAD 5-36V				500000339
U8-9	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL 741C				500001458

Table 8—15. MF Detector A7 Parts List.

REV 09 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
C1	CAPACITR	POLYSTYR	22	NF	CAP.018	N	100V	2%	.022	UF	321502230
C2-3	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C4	CAPACITR	POLYSTYR	22	NF	CAP.018	N	100V	2%	.022	UF	321502230
C5	CAPACITR	CERAMIC	10	PF	CAP.082		1KV	10%	N330		330001000
C6	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027	UF	322902741
C7-10	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C11-13	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027	UF	322902741
C14	CAPACITR	POLYESTR	150	NF		N	250V	10%	.15	UF	320215421
C15	CAPACITR	CERAMIC	10	PF	CAP.082		1KV	10%	N330		330001000
C16-17	CAPACITR	ELECT-NP	4.7	UF	CAP.032	N	25V	-10	+100%	N-P	301304750
C18-25	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C26-27	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027	UF	322902741
C28-29	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C30-31	CAPACITR	ELECT-TA	10	UF	CAP.032	N	20V	10%			310301060
C32-33	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027	UF	322902741
C34-36	CAPACITR	ELECT-TA	10	UF	CAP.042	N	20V	20%			310801060
C37	CAPACITR	POLYESTR	150	NF		N	250V	10%	.15	UF	320215421
C38-39	CAPACITR	CERAMIC	680	PF	CAP.082		1KV	10%	Z5R		330006810
C40	CAPACITR	CERAMIC	220	NF	CAP.037		50V	20%	Y5V.22	UF	330802240
CR1-2	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS		560041480
CR5-12	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS		560041480
R1-3	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			200001046
R4-6	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R7-8	RESISTOR	MTL-FILM	82.5	K	RES.001	P	1/8W	1%	100PPMRN55		220282521
R9	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			200001046
R10	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R11	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			200001046
R12	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R13	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			200001046
R14-16	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R17-19	RESISTOR	MTL-FILM	4.53	K	RES.001	N	1/8W	.25	50PPM-RN55		222145310
R20-22	RESISTOR	MTL-FILM	28.0	K	RES.001	P	1/8W	1%	100PPMRN55		220228021
R23	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R24	RESISTOR	MTL-FILM	5.36	K	RES.001	P	1/8W	1%	100PPMRN55		220253611
R25	RESISTOR	MTL-FILM	64.9	K	RES.001	P	1/8W	1%	100PPMRN55		220264921
R26	TRIM-POT	CERM-15T	20	K	VRES.001	P	3/4W	10%	END-ADJ		232502030
R27-28	RESISTOR	MTL-FILM	5.36	K	RES.001	P	1/8W	1%	100PPMRN55		220253611
R29	RESISTOR	MTL-FILM	4.53	K	RES.001	N	1/8W	.25	50PPM-RN55		222145310
R30	RESISTOR	MTL-FILM	59.0	K	RES.001	P	1/8W	1%	100PPMRN55		220259021
R31-33	RESISTOR	MTL-FILM	5.36	K	RES.001	N	1/8W	.25	100PPMRN55		220453618
R34	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R35	RESISTOR	MTL-FILM	34.0	K	RES.001	P	1/8W	1%	100PPMRN55		220234021
R36	RESISTOR	MTL-FILM	7.15	K	RES.001	P	1/8W	1%	100PPMRN55		220271511
R37-39	RESISTOR	MTL-FILM	28.0	K	RES.001	P	1/8W	1%	100PPMRN55		220228021
R40	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R41-46	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55		220210021
R47	TRIM-POT	CERM-15T	1.0	K	VRES.001	P	3/4W	10%	END-ADJ		232501020
R48	RESISTOR	MTL-FILM	4.87	K	RES.001	P	1/8W	1%	100PPMRN55		220248711
R49	RESISTOR	MTL-FILM	4.02	K	RES.001	P	1/8W	1%	100PPMRN55		220240211
R50	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R51	RESISTOR	MTL-FILM	5.36	K	RES.001	N	1/8W	.25	100PPMRN55		220453618
R52	RESISTOR	MTL-FILM	59.0	K	RES.001	P	1/8W	1%	100PPMRN55		220259021
R53	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R54	RESISTOR	MTL-FILM	34.0	K	RES.001	P	1/8W	1%	100PPMRN55		220234021
R55	RESISTOR	MTL-FILM	7.15	K	RES.001	P	1/8W	1%	100PPMRN55		220271511
R56	RESISTOR	MTL-FILM	499	R	RES.001	P	1/8W	1%	100PPMRN55		220249901
R57	RESISTOR	MTL-FILM	2.05	K	RES.001	P	1/8W	1%	100PPMRN55		220220511
R58	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036

Table 8—15. (Cont'd.)

REV 09 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
R59	RESISTOR	MTL-FILM	499	R	RES.001	P	1/8W	1%	100PPMRN55		220249901
R60	RESISTOR	MTL-FILM	2.05	K	RES.001	P	1/8W	1%	100PPMRN55		220220511
R61-62	RESISTOR	MTL-FILM	4.53	K	RES.001	P	1/8W	1%	100PPMRN55		220245311
R63	TRIM-POT	CERM-15T	20	K	VRES.001	P	3/4W	10%	END-ADJ		232502030
R64	TRIM-POT	CERM-15T	1.0	K	VRES.001	P	3/4W	10%	END-ADJ		232501020
R65	RESISTOR	MTL-FILM	64.9	K	RES.001	P	1/8W	1%	100PPMRN55		220264921
R66	RESISTOR	MTL-FILM	4.53	K	RES.001	P	1/8W	1%	100PPMRN55		220245311
R67-68	RESISTOR	MTL-FILM	499	K	RES.001	P	1/8W	1%	100PPMRN55		220249931
U1	INT-CKT	CMOS	4538BUF	DIP.16	P	2X	PRC	MONO	MLTIVI		510004538
U2	INT-CKT	CMOS	4093BUF	DIP.14	P	4X2	IN	NAND	SCHM TR		510004093
U3-6	INT-CKT	OP-AMP	1458	DIP.8	P	DUAL	741C				500001458
U7	INT-CKT	COMPARTR	339	DIP.14	P	QUAD	5-36V				500000339
U8-9	INT-CKT	OP-AMP	1458	DIP.8	P	DUAL	741C				500001458

Table 8—16. MF Detector A8 Parts List.

REV 10 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
C1	CAPACITR	POLYSTYR	22	NF	CAP.018	N	100V	2%	.022 UF		321502230
C2-3	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C4	CAPACITR	POLYSTYR	22	NF	CAP.018	N	100V	2%	.022 UF		321502230
C5	CAPACITR	CERAMIC	10	PF	CAP.082		1KV	10%	N330		3300001000
C6	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027 UF		322902741
C7-10	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C11-13	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027 UF		322902741
C14	CAPACITR	POLYESTR	150	NF		N	250V	10%	.15 UF		320215421
C15	CAPACITR	CERAMIC	10	PF	CAP.082		1KV	10%	N330		3300001000
C16-17	CAPACITR	ELECT-NP	4.7	UF	CAP.032	N	25V	-10	+100% N-P		301304750
C18-25	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C26-27	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027 UF		322902741
C28-29	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
C30-31	CAPACITR	ELECT-NP	10	UF	CAP.029	N	25V	-10	+100% N-P		301301060
C32-33	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V	1%	.027 UF		322902741
C34-36	CAPACITR	ELECT-TA	10	UF	CAP.042	N	20V	20%			310801060
C37	CAPACITR	POLYESTR	150	NF		N	250V	10%	.15 UF		320215421
C38-39	CAPACITR	CERAMIC	680	PF	CAP.082		1KV	10%	Z5R		330006810
C40	CAPACITR	CERAMIC	220	NF	CAP.037		50V	20%	Y5V.22	UF	330802240
CR1-2	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS		560041480
CR5-12	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS		560041480
R1-3	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			2000001046
R4-6	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			2000001036
R7-8	RESISTOR	MTL-FILM	82.5	K	RES.001	P	1/8W	1%	100PPMRN55		220282521
R9	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			2000001046
R10	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			2000001036
R11	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			2000001046
R12	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			2000001036
R13	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%			2000001046
R14-16	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			2000001036
R17-19	RESISTOR	MTL-FILM	3.48	K	RES.001	N	1/8W	.25	50PPM-RN55		222134810
R20-22	RESISTOR	MTL-FILM	28.0	K	RES.001	P	1/8W	1%	100PPMRN55		220228021
R23	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R24	RESISTOR	MTL-FILM	3.92	K	RES.001	P	1/8W	1%	100PPMRN55		220239211

Table 8-16. (Cont'd.)

REV 10 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
R25	RESISTOR	MTL-FILM	64.9	K	RES.001	P	1/8W	1%	100PPMRN55		220264921
R26	TRIM-POT	CERM-1ST	20	K	VRES.001	P	3/4W	10%	END-ADJ		232502030
R27-28	RESISTOR	MTL-FILM	3.92	K	RES.001	P	1/8W	1%	100PPMRN55		220239211
R29	RESISTOR	MTL-FILM	3.48	K	RES.001	N	1/8W	.25	50PPM-RN55		222134810
R30	RESISTOR	MTL-FILM	59.0	K	RES.001	P	1/8W	1%	100PPMRN55		220259021
R31-33	RESISTOR	MTL-FILM	3.92	K	RES.001	N	1/8W	.25	50PPM-RN55		222139210
R34	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R35	RESISTOR	MTL-FILM	34.0	K	RES.001	P	1/8W	1%	100PPMRN55		220234021
R36	RESISTOR	MTL-FILM	7.15	K	RES.001	P	1/8W	1%	100PPMRN55		220271511
R37-39	RESISTOR	MTL-FILM	28.0	K	RES.001	P	1/8W	1%	100PPMRN55		220228021
R40	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R41-46	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55		220210021
R47	TRIM-POT	CERM-1ST	1.0	K	VRES.001	P	3/4W	10%	END-ADJ		232501020
R48	RESISTOR	MTL-FILM	3.40	K	RES.001	P	1/8W	1%	100PPMRN55		220234011
R49	RESISTOR	MTL-FILM	2.94	K	RES.001	P	1/8W	1%	100PPMRN55		220229411
R50	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R51	RESISTOR	MTL-FILM	3.92	K	RES.001	N	1/8W	.25	50PPM-RN55		222139210
R52	RESISTOR	MTL-FILM	59.0	K	RES.001	P	1/8W	1%	100PPMRN55		220259021
R53	RESISTOR	MTL-FILM	14.0	K	RES.001	P	1/8W	1%	100PPMRN55		220214021
R54	RESISTOR	MTL-FILM	34.0	K	RES.001	P	1/8W	1%	100PPMRN55		220234021
R55	RESISTOR	MTL-FILM	7.15	K	RES.001	P	1/8W	1%	100PPMRN55		220271511
R56	RESISTOR	MTL-FILM	499	R	RES.001	P	1/8W	1%	100PPMRN55		220249901
R57	RESISTOR	MTL-FILM	2.05	K	RES.001	P	1/8W	1%	100PPMRN55		220220511
R58	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R59	RESISTOR	MTL-FILM	499	R	RES.001	P	1/8W	1%	100PPMRN55		220249901
R60	RESISTOR	MTL-FILM	2.05	K	RES.001	P	1/8W	1%	100PPMRN55		220220511
R61-62	RESISTOR	MTL-FILM	3.48	K	RES.001	P	1/8W	1%	100PPMRN55		220234811
R63	TRIM-POT	CERM-1ST	20	K	VRES.001	P	3/4W	10%	END-ADJ		232502030
R64	TRIM-POT	CERM-1ST	1.0	K	VRES.001	P	3/4W	10%	END-ADJ		232501020
R65	RESISTOR	MTL-FILM	64.9	K	RES.001	P	1/8W	1%	100PPMRN55		220264921
R66	RESISTOR	MTL-FILM	3.48	K	RES.001	P	1/8W	1%	100PPMRN55		220234811
R67-68	RESISTOR	MTL-FILM	499	K	RES.001	P	1/8W	1%	100PPMRN55		220249931
S3	PB, IMPS	SERIES			SPST		P/P				635800702
S5-6	PB, IMPS	SERIES			SPST		P/P				635800702
U1	INT-CKT	CMOS	4538BUF	DIP.16	P	2X	PRC	MONO	MLTIVI		510004538
U2	INT-CKT	CMOS	4093BUF	DIP.14	P	4X2	IN	NAND	SCHM TR		510004093
U3-6	INT-CKT	OP-AMP	1458	DIP.8	P	DUAL	741C				500001458
U7	INT-CKT	COMPARTR	339	DIP.14	P	QUAD	5-36V				500000339
U8-9	INT-CKT	OP-AMP	1458	DIP.8	P	DUAL	741C				500001458

Table 8-17. DTMF Receiver A6 Parts List.

REV 15 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
C1-2	CAPACITR	T-P-PROP	150	NF	CAP.027	N	100V	1%	.15	UF	322401541
C4	CAPACITR	CERAMIC	100	PF	CAP.082		1KV	10%	N3300		330001010
C5-6	CAPACITR	CERAMIC	10	NF	CAP.088		50V	10%	W5R.010	UF	330801030
C7	CAPACITR	CERAMIC	100	PF	CAP.082		1KV	10%	N3300		330001010
C9-10	CAPACITR	CERAMIC	10	NF	CAP.088		50V	10%	W5R.010	UF	330801030
C12	CAPACITR	CERAMIC	10	NF	CAP.088		50V	10%	W5R.010	UF	330801030
C13-14	CAPACITR	A-P-PROP	10	NF	CAP.059	P	100V	1%	.010	UF	322401030
C19-20	CAPACITR	CERAMIC	100	PF	CAP.082		1KV	10%	N3300		330001010
C31-33	CAPACITR	ELECT-TA	22	UF	CAP.037	N	15V	10%			310002261

Table 8-17. (Cont'd.)

REV 15 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
C34-35	CAPACITR	A-P-PROP	10	NF	CAP.059	P	100V	1%	.010 UF	322401030	
C36-37	CAPACITR	SIL-MICA	820	PF	CAP.093	N	300V	5%		335408210	
C38-39	CAPACITR	ELECT-TA	1.5	UF	CAP.036	P	35V	10%		310001551	
C41-42	CAPACITR	CERAMIC	4.7	NF	CAP.088		50V	10%	WSR4700 PF	330804720	
C44-47	CAPACITR	CERAMIC	100	NF	CAP.037		50V	10%	WSR.1 UF	330801041	
C48-50	CAPACITR	SIL-MICA	10	PF	CAP.091	N	100V	5%		335401000	
C51-52	CAPACITR	CERAMIC	100	NF	CAP.037		50V	10%	WSR.1 UF	330801041	
CR1-6	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS	560041480	
R1	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%		200001036	
R2	RESISTOR	CARBON	1.8	K	RES.001	P	1/4W	10%		200101826	
R3	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%		200001036	
R4-5	RESISTOR	MTL-FILM	10.5	K	RES.001	P	1/8W	1%	100PPMRN55	220210521	
R6	RESISTOR	MTL-FILM	1.30	K	RES.001	P	1/8W	1%	100PPMRN55	220213011	
R7	RESISTOR	MTL-FILM	2.55	K	RES.001	P	1/8W	1%	100PPMRN55	220225511	
R8	RESISTOR	MTL-FILM	11.5	K	RES.001	P	1/8W	1%	100PPMRN55	220214591	
R9-10	RESISTOR	MTL-FILM	174	K	RES.001	P	1/8W	1%	100PPMRN55	220217431	
R11-12	RESISTOR	CARBON	100	K	RES.001	N	1/8W	10%		200001046	
R13	RESISTOR	MTL-FILM	301	K	RES.001	P	1/8W	1%	100PPMRN55	220230131	
R14	RESISTOR	MTL-FILM	200	K	RES.001	P	1/8W	1%	100PPMRN55	220220031	
R15-16	RESISTOR	MTL-FILM	806	K	RES.001	P	1/8W	1%	100PPMRN55	220280631	
R17-18	RESISTOR	MTL-FILM	221	K	RES.001	P	1/8W	1%	100PPMRN55	220222131	
R19-20	RESISTOR	MTL-FILM	28.7	K	RES.001	P	1/8W	1%	100PPMRN55	220228721	
R21-22	RESISTOR	MTL-FILM	1.00	M	RES.001	P	1/8W	1%	100PPMRN55	220210041	
R23-24	RESISTOR	CARBON	2.7	M	RES.001	P	1/4W	10%		200102756	
R25-27	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%		200001036	
R28	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55	220210021	
R29	RESISTOR	MTL-FILM	4.12	K	RES.001	P	1/8W	1%	100PPMRN55	220241211	
R30-31	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W	1%	100PPMRN55	220210021	
R32-33	RESISTOR	MTL-FILM	1.00	M	RES.001	P	1/8W	1%	100PPMRN55	220210041	
R34	RESISTOR	CARBON	1.5	K	RES.001	P	1/4W	10%		200101526	
R35	RESISTOR	CARBON	1.0	M	RES.001	P	1/4W	10%		200101056	
U1	RESISTOR	NETWORK	8X10K		DIP.16		100V	2%		514500102	
U2	INT-CKT	CMOS	4538BUF		DIP.16	P	2X	PRC	MONO MLTIV1	510004538	
U3	RESISTOR	NETWORK	8X10K		DIP.16		100V	2%		514500102	
U4	INT-CKT	CMOS	4016BUF		DIP.14	P	4	BILAT	SWITCH	510004016	
U5	INT-CKT	COMPARTR	339		DIP.14	P		QUAD	5-36V	500000339	
U6	INT-CKT	CMOS	4538BUF		DIP.16	P	2X	PRC	MONO MLTIV1	510004538	
U7	INT-CKT	CMOS	4016BUF		DIP.14	P	4	BILAT	SWITCH	510004016	
U8	INT-CKT	OP-AMP	1458		DIP.8	P		DUAL	741C	500001458	
U9	INT-CKT	CMOS	4023		DIP.14	P		3X3	IN NAND GTE	510004023	
U10	INT-CKT	CMOS	4011BUF		DIP.14	P		4X2	IN NAND GATE	510004011	
U11	INT-CKT	FILTER	CH1295					BNDPAS	TCH/TON ACTV	514001310	
U12	RESISTOR	NETWORK	7X10K		RESNET.8		100V	2%		514500010	
U13	INT-CKT	DTMF-REC	CRC8030							567000701	
U14	INT-CKT	CMOS	4069		DIP.14	P		HEX	INVERTER	510004069	
U15	INT-CKT	FILTER	CH1296					BNDPAS	TCH/TON ACTV	514001311	
U16-17	INT-CKT	CMOS	4053BUF		DIP.16	P		3X2CHN	ALG MUX/DEMU	510004053	
U18	INT-CKT	CMOS	4011BUF		DIP.14	P		4X2	IN NAND GATE	510004011	
Y1	CRYSTAL	FUND-PAR	3.5795M		HC-18		50PPM	18PF	200R	919100017	

Table 8-18. Dither Generator and Control A6 Parts List.

REV 02 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION							PART NO.
C1-3	CAPACITR	ELECT-TA	22	UF	CAP.037	N	15V 10%	310002261
C4-5	CAPACITR	CERAMIC	100	PF	CAP.082		1KV 10% N3300	330001010
C6-7	CAPACITR	CERAMIC	10	NF	CAP.088		50V 10% W5R.010 UF	330801030
C8-10	CAPACITR	CERAMIC	10	NF	CAP.082		16V 20% Y5P.010 UF	330701031
R1	RESISTOR	CARBON	10	K	RES.001	N	1/8W 10%	200001036
R2	RESISTOR	MTL-FILM	10.0	K	RES.001	P	1/8W 1% 100PPMRN55	220210021
R3	RESISTOR	MTL-FILM	4.12	K	RES.001	P	1/8W 1% 100PPMRN55	220241211
R4	RESISTOR	MTL-FILM	1.30	K	RES.001	P	1/8W 1% 100PPMRN55	220213011
R5	RESISTOR	MTL-FILM	2.55	K	RES.001	P	1/8W 1% 100PPMRN55	220225511
R6	RESISTOR	MTL-FILM	11.5	R	RES.001	P	1/8W 1% 100PPMRN55	220211591
U1	INT-CKT	CMOS	4022BUF	DIP.16	P	OC TL CNTR W/B OUT		510004022
U2	INT-CKT	CMOS	4013BUF	DIP.14	P	2 D FLP-FLP		510004013
U3	INT-CKT	OP-AMP	1458	DIP.8	P	DUAL 741C		500001458
U4	INT-CKT	CMOS	4016BUF	DIP.14	P	4 BILAT SWITCH		510004016

Table 8-19. CDA Interface A10 Parts List.

REV 08 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION							PART NO.
C1-11	CAPACITR	CERAMIC	10	NF	CAP.082		16V 20% Y5P.010 UF	330701031
C12	CAPACITR	CERAMIC	10	NF	CAP.088		50V 00 Z5U.010 UF	330801031
C14	CAPACITR	CERAMIC	10	NF	CAP.082		16V 20% Y5P.010 UF	330701031
C15	CAPACITR	ELECT-TA	22	UF	CAP.039	N	35V 20%	310802261
C16	CAPACITR	CERAMIC	100	NF	CAP.085		75V 00 Z5V.1 UF	330201040
CR1	DIODE	SIGNAL	1N4148	DIO.001			75V SI 4.0NS	560041480
J1	CONNECTR	HEADER	26 DIL	!			GOLD STRAIT W/LCK	654003713
K1	RELAY	SEALED	6V 2C	!			AU 2A 60R PC	604102750
Q1	TRANSSTR	BJT-PNP	2N3905	T092.01			40V SI HFES0 200MA	552039050
R1	RESISTOR	MTL-FILM	14.3	K	RES.001	P	1/8W 1% 100PPMRN55	220214321
R5	RESISTOR	CARBON	1.0	K	RES.001	P	1/4W 10%	200101026
R6	RESISTOR	CARBON	390	R	RES.001	N	1/8W 10%	200003916
R7	RESISTOR	CARBON	10	K	RES.001	P	1/4W 10%	200101036
RN1-3	RESISTOR	NETWORK	7X1K	RESNET.8			100V 2%	514500002
U1-6	INT-CKT	TTL	7401	DIP.14	N	4X2 IN NAND GATE/OC		510074010
U7	INT-CKT	TTL	7404	DIP.14	N	HEX INVERTER		510074040
U8-10	INT-CKT	LS-TTL	74LS175	DIP.16	P	4 D EDGE-TRIG F/F		510974175
U11	INT-CKT	TTL	74121	DIP.14	N	MONO MULTIVIB		510074121
U12	INT-CKT	LS-TTL	74LS01	DIP.14	P	4X2 IN NAND GT /OC		510907401

Table 8-20. External Alarm Relay Driver A10 Parts List.

REV 00 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
C1	CAPACITR	ELECT-TA	22	UF	CAP.039	N	35V	20%			310802261
C2	CAPACITR	CERAMIC	100	NF	CAP.085		75V	00	Z5V.1	UF	330201040
C3	CAPACITR	CERAMIC	10	NF	CAP.082		16V	20%	YSP.010	UF	330701031
CR1	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS		560041480
K1	RELAY	SEALED	6V 2C	!			AU	2A	60R	PC	604102750
Q1	TRANSSTR	BJT-PNP	2N3905		T092.01		40V	SI	HFE50	200MA	552039050
R1	RESISTOR	CARBON	10	K	RES.001	P	1/4W	10%			200101036
R2	RESISTOR	CARBON	390	R	RES.001	P	1/4W	10%			200103916
R3	RESISTOR	CARBON	1.0	K	RES.001	P	1/4W	10%			200101026
U1	INT-CKT	LS-TTL	74LS01		DIP.14	P	4X2	IN	NAND	GT /OC	510907401

Table 8-21. Microprocessor A11 Parts List.

REV 15 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION										PART NO.
C1-5	CAPACITR	CERAMIC	10	NF	CAP.082		16V	20%	YSP.010	UF	330701031
C6	CAPACITR	ELECT-TA	22	UF	CAP.039	N	25V	20%			310402260
C7-8	CAPACITR	CERAMIC	20	PF	CAP.082		1KV	10%	N330		330002000
C9	CAPACITR	ELECT-TA	1.0	UF	CAP.036	P	35V	10%			310001051
C10-23	CAPACITR	CERAMIC	10	NF	CAP.082		16V	20%	YSP.010	UF	330701031
C24	CAPACITR	POLYSTYR	10	NF	CAP.018	N	100V	1%	.010	UF	321501031
C25	CAPACITR	SIL-MICA	100	PF	CAP.091	P	500V	2%			335401010
C26	CAPACITR	CERAMIC	56	PF	CAP.082		1KV	10%	N3300		330005600
C27-28	CAPACITR	CERAMIC	10	NF	CAP.082		16V	20%	YSP.010	UF	330701031
C29	CAPACITR	SIL-MICA	100	PF	CAP.091	P	500V	2%			335401010
C30	CAPACITR	T-P-PROP	470	NF	CAP.076	N	100V	1%	.47	UF	322304741
C31	CAPACITR	CERAMIC	100	NF	CAP.088		50V	20%	X5V.1	UF	330801040
CR5-6	DIODE	SIGNAL	1N4148		DIO.001		75V	SI	4.0NS		560041480
Q1-2	TRANSSTR	BJT-NPN	MPS6515		T092.01		25V	SI	HFE250	0.1A	550065150
R1-4	RESISTOR	CARBON	2.2	M	RES.001	N	1/8W	10%			200002256
R5	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R6	RESISTOR	CARBON	56	R	RES.001	P	1/4W	10%			200105606
R7	TRIM-POT	CERM-1ST	20	K	VRES.001	P	3/4W	10%	END-ADJ		232502030
R8	RESISTOR	MTL-FILM	90.9	K	RES.001	P	1/8W	1%	100PPMRN55		220290921
R9	RESISTOR	MTL-FILM	61.9	K	RES.001	P	1/8W	1%	100PPMRN55		220261921
R10	RESISTOR	MTL-FILM	249	K	RES.001	P	1/8W	1%	100PPMRN55		220224931
R11	RESISTOR	CARBON	2.2	M	RES.001	N	1/8W	10%			200002256
R12	RESISTOR	MTL-FILM	34.0	K	RES.001	P	1/8W	1%	100PPMRN55		220234021
R13	RESISTOR	MTL-FILM	200	K	RES.001	P	1/8W	1%	100PPMRN55		220220031
R18-20	RESISTOR	CARBON	10	K	RES.001	N	1/8W	10%			200001036
R22-23	RESISTOR	CARBON	100	K	RES.001	P	1/4W	10%			200101046
R24	RESISTOR	CARBON	1.0	K	RES.001	P	1/4W	10%			200101026
R26	RESISTOR	CARBON	10	K	RES.001	P	1/4W	10%			200101036
R27	RESISTOR	CARBON	1.0	M	RES.001	P	1/4W	10%			200101056
U1	RESISTOR	NETWORK	13X2K		DIP.14		100V	2%			514500100
U2	INT-CKT	CMOS	4001BUF		DIP.14	P	4X2	IN	NOR	GATE	510004001
U4	INT-CKT	LS-TTL	74LS00		DIP.14	P	4X2	IN	NAND	GATE	510907400

Table 8-21. (Cont'd.)

REV 15 DATED 6/30/82

REFERENCE DESIGNATOR	DESCRIPTION						PART NO.
U5	INT-CKT	LS-TTL	74LS04	DIP.14	P	HEX INVERTER	510907404
U6	INT-CKT	CMOS	4071	DIP.14	P	4X2 IN OR GTE	510004071
U7	RESISTOR	NETWORK	8X10K	DIP.16		100V 2%	514500102
U8	INT-CKT	CMOS	4051BUF	DIP.16	P	8CHN ANL MUX/DEMUX	510004051
U10	INT-CKT	MEMORY	2101A-2	DIP.22		256 X 4 NMOS	514000405
U11	INT-CKT	CMOS	4013BUF	DIP.14	P	2 D FLP-FLP	510004013
U12-15	INT-CKT	CMOS	4076BUF	DIP.16	P	4 D F-F REGISTER	510004076
U16	INT-CKT	MEMORY	2101A-2	DIP.22		256 X 4 NMOS	514000405
U17-20	INT-CKT	CMOS	4076BUF	DIP.16	P	4 D F-F REGISTER	510004076
U21-22	INT-CKT	CMOS	4510BUF	DIP.16	P	BCD U/D PRSET CNTR	510004510
U23-24	INT-CKT	CMOS	4538BUF	DIP.16	N	2X PREC MONO MULTV8	510014538
XU2	SOCKET	PC MOUNT	14 DIL	!		.300 .150HT TIN	820100300
XU9	SOCKET	PC MOUNT		!			820101400
XU25	SOCKET, IC	PC, LOW PROFILE		24D1LP			820101500

ADDENDUM TO 2763-00 MANUAL

ADDENDUM #1

For the units with serial numbers above 1471 the DTMF Receiver Board (A6), the following specification apply:

TWIST (MF/DTMF)

(twist = level difference of tones in a compound signal...high frequency level with respect to low frequency level.)

COMPOUND LEVEL -20 to +2 dBm:

MF		DTMF		
-----		-----		
accept	reject	accept		reject
+/-6dB	+/-15dB	+4dB	-8dB	not
	typical			specified

(MF: F1 and F2 +/-1% of nominal frequency)

(DTMF: F1 and F2 +/-1.5% of nominal frequency)

CIRCUIT DESCRIPTION

2.1 GENERAL

The heart of the circuit is the DTMF six pole switched capacitor filter and the DTMF decoder chips, which are programed for 2/8 outputs.

2.2 MGC/AGC CONTROL

The input signal takes two paths, one of which is through the manual gain control (MGC) circuit. The signal is presented to the RMS to DC converter, which converts both AC and DC input components to the input signal, the converter is DC blocked. The converter output is range attenuated and compared to a DC level which is user-selectable according to the position of the receiver level potentiometer on the front panel of the instrument. Positive feedback is provided to the comparator from a combination of the comparator output and the strobe output from the decoders. The comparator output is logically anded with the MF/DTMF control line and used to gate valid strobe pulses to the MF/DTMF data selectors. When valid power levels are detected by the MGC circuit, the positive feedback latches the comparator; if the strobe pulse subsequently becomes active signifying that one or more DTMF tones have been detected, the comparator is continuously latched until both input and strobe become idle. When the instrument is in the automatic gain control (AGC) mode, the output of the RMS to DC converter is compared to a minimum DC voltage, allowing the filter chip to accept any tone within its dynamic range.

2.3 DTMF FILTER CHIP

The second input signal path is through the DTMF filter chip via an attenuator pad (approximately 10dB), which limits the specified dynamic range of the input to the guaranteed minimum dynamic range of the filter chip. The high band and low band outputs of the filter present square wave signals at the frequency(ies) detected in each band at the input.

2.4 DTMF DECODER CONTROL

The filter outputs are connected to three DTMF decoder chips, which generate a strobe signal when a valid pair of DTMF tones has been detected. Both filter outputs are connected to the first decoder, which therefore, presents a strobe pulse only when the input signal is composed of exactly one tone from each band. Since single tone detection is an instrument feature, the second and third decoders are presented with, respectively, the low and high band outputs from the filter and high and low band single frequencies from on board oscillators. Steering logic enables transmission gates to pass the oscillator outputs to the second and third decoder chips only when no valid two-tone combination is present to activate the first decoder. If a valid pair of tones are not present, the first decoder is never stimulated and the transmission gates are always enabled. If a valid tone pair is present, the EST (early steering output) lead disables the transmission gates about 14 milliseconds before any strobe output becomes active. The error function control lead activates the single tone oscillators only when the error function has been selected externally.

2.5 DECODER OUTPUTS

The tri-state outputs of the three decoders are bussed together; the steering logic prevents the outputs of more than one decoder from going active at any given time. The timing components of the three decoders are designed to create strobe pulses which represent the pulse width of the input signal less 14 milliseconds (since the tone present time is incremented by 14 milliseconds by the microprocessor on another assembly).

2.6 OSCILLATOR TUNING

The single tone oscillators are equipped with potentiometers which enable fine tuning of center frequencies, overcoming component value tolerances. Subsequent changes of center frequencies due to temperature-induced component value changes will be within the bandwidth of the decoder chips.

2.7 DATA SELECTORS

The output data selectors pass MF signals through the assembly when the DTMF/MF control lead is low. When this control lead is high, the input level is adequate, and DTMF tones have been detected, the decoder outputs are passed through the data selectors. When only the DTMF tone has been detected and the error function is enabled, only the appropriate high or low group data selector is enabled.

2.8 DITHER SIGNAL GENERATOR

Sensitivity control for MF detectors (which are located on another assembly) is determined by the REC level lead, which is modified by chopping at 12.85 KHZ and 3 DB of gain.

